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RESEARCH INTERESTS

Compilers and Programming Languages
Systems in High-Performance Computing
Computer Architectures

EDUCATION

Ph.D. in Computer Science, University of Illinois at Urbana-Champaign 8/95 – 10/99
Thesis: Compilation Techniques for Explicitly Parallel Programs
Advisor: David A. Padua

M.S. in Computer Science, Stanford University 9/93 – 6/95

B.S. in Physics, Seoul National University, Seoul, Korea 3/86 – 2/91

EXPERIENCE

Assistant Professor	Department of Computer Science and Engineering, Michigan State University, East Lansing, Michigan	1/00 – present
Visiting Lecturer	Department of Computer Science, University of Illinois at Urbana-Champaign	8/99 – 12/99
Postdoc.	Department of Computer Science, University of Illinois at Urbana-Champaign	8/99 – 12/99
Summer Intern	IBM T. J. Watson Research Center, New York	6/97 – 8/97
Research Assistant	Department of Computer Science, University of Illinois at Urbana-Champaign	1/97 – 8/99
Research Assistant	Center for Supercomputing Research and Development, University of Illinois at Urbana-Champaign	1/96 – 12/97
Teaching Assistant	Department of Computer Science, University of Illinois at Urbana-Champaign	8/95 – 12/95
Teaching Assistant	Department of Computer Science, Stanford University	1/95 – 6/95
Research Assistant	Department of Computer Science, Stanford University	9/94 – 3/95

HONORS and AWARDS

Best Paper Award,
5th Workshop on Multithreaded Execution, Architecture, and Compilation Dec. 2001
IBM Cooperative Fellowship Aug. 1997 – May 1999
Korea Foundation for Advanced Studies Scholarship Sep. 1997 – Aug. 1999
Phi Kappa Phi

GRANTS

"An Optimizing Compiler for Languages with Programmable Memory Models",
Information Technology Research Program, CCR-0081265, *The National Science Foundation*
with Samuel P. Midkiff and David A. Padua
$499,387, Sep. 2000 - Aug. 2003.

"A Proxy Centric Testbed for Mobile Internet Research",
CISE Research Resources Program, EIA-0130724, *The National Science Foundation*
with Betty H.Cheng, Laura Dillon, Sandeep S. Kulkarni, Philip K. McKinley, and Kurt Stirewalt
$96,390, Jan. 2002 - Dec. 2004.

PROFESSIONAL ACTIVITIES

Program committee member of
ISPAN'02: The 6th International Symposium on Parallel Architectures, Algorithms, and Networks
JVM'02: The 2nd USENIX Java Virtual Machine Research and Technology Symposium

Referee for
IEEE Transactions on Computers
IEEE Transactions on Parallel and Distributed Systems
Journal of Parallel and Distributed Computing
IEE Proceedings Part E: Computers and Digital Techniques
International Journal of Parallel Programming
Theoretical Computer Science
ACM Java Grande Conference
International Conference on Parallel Architectures and Compilation Techniques
International Symposium on High-Performance Computer Architecture
International Parallel and Distributed Processing Symposium
International Conference on Parallel Processing
International Conference on Compiler Construction
Workshop on Languages and Compilers for Parallel Computing
Euro-Par Conference
Euromicro Workshop on Parallel and Distributed Processing

Member of IEEE and ACM.

DEPARTMENTAL ACTIVITIES

Graduate Studies and Research Committee — Fall 2000 - present

COURSES TAUGHT

Graduate Courses Taught

CSE 891	*Advanced Program Analysis and Optimization Techniques*, Michigan State University	Fall 2001
CSE 822	*Parallel Processing Computer Systems*, Michigan State University	Spring 2001

COURSES TAUGHT (continued)

Undergraduate Courses Taught

CSE 450	*Translation of Programming Languages*, Michigan State University	Spring 2002
CSE 320	*Computer Organization and Assembly Language Programming*, Michigan State University (37 undergraduate and 2 graduate students)	Fall 2000
CSE 450	*Translation of Programming Languages*, Michigan State University (13 undergraduate and 5 graduate students)	Spring 2000
CS 231	*Computer Architecture I*, University of Illinois at Urbana-Champaign (184 undergraduate students)	Fall 1999
CS 296	*Honors Course in Computer Science*, University of Illinois at Urbana-Champaign (6 undergraduate students)	Fall 1999

STUDENT RESEARCH SUPERVISION

Current Dotoral Students

Min Deng
Yan Solihin (co-advising with Prof. Josep Torrellas, University of Illinois at Urbana-Champaign)
Ji Zhang

Current Masters Students

Xing Fang
Kapila Moonesinghe

INVITED TALKS

"An Optimizing Compiler for Relaxed Memory Consistency Models"

Department of Computer Science, University of Massachusetts at Amherst, Massachusetts	Feb. 2001
Department of Computer Science, Northwestern University, Illinois	Feb. 2001
Department of Computer Science, State University of New York at Stony Brook, New York	Mar. 2001
Department of Computer Science, Boston University, Massachusetts	Mar. 2001

"Automatically Mapping Code on an Intelligent Memory Architecture"

Department of Electrical and Computer Engineering, Northwestern University, Illinois	Feb. 2001

"Compilation Techniques for Explicitly Parallel Programs"

Dagstuhl Seminar 00341, Schloss Dagstuhl, Wadern, Germany	Aug. 2000
School of Computer Science and Engineering, Seoul National University, Korea	May 2000
Department of Electrical and Computer Engineering, University of Toronto, Canada	Jul. 1999
Star Core, Atlanta, Georgia	Jun. 1999
Intel, Santa Clara, California	Apr. 1999
Sun Microsystems, Mountain View, California	Apr. 1999
Hewlett Packard, Cupertino, California	Apr. 1999
Department of Computer Science, University of Rochester, New York	Mar. 1999
Department of Computer Science and Engineering, Michigan State University, Michigan	Mar. 1999
Department of Computer Science, Florida State University, Tallahassee, Florida	Mar. 1999

CONFERENCE and WORKSHOP PRESENTATIONS

"An Optimizing Compiler for Languages with Programmable Memory Models", Birds-of-a-Feather on Using Jalapeño as a Research VM (ACM SIGPLAN 2001 Conference on Programming Language Design and Implementation), Snowbird, Utah, Jun. 2001

"Automatically Mapping Code on an Intelligent Memory Architecture", 7th International Symposium on High Performance Computer Architecture (HPCA), Monterrey, Mexico, Jan. 2001

"Hiding Relaxed Memory Consistency with Compilers", 2000 International Conference on Parallel Architectures and Compilation Techniques (PACT), Philadelphia, Pennsylvania, Oct. 2000.

"Hiding the Java Memory Model with Compilers", OOPSLA workshop: Revising the Java Thread Specification (`http://www.cs.umd.edu/~pugh/java/memoryModel/workshop`), Twin Cities, Minnesota, Oct. 2000

"Basic Compiler Algorithms for Parallel Programs", 7th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), Atlanta, Georgia, May 1999.

"Concurrent Static Single Assignment Form and Constant Propagation for Explicitly Parallel Programs", 10th International Workshop on Languages and Compilers for Parallel Computing (LCPC), Twin Cities, Minnesota, Aug. 1997.

"Parallel Static Single Assignment Form and Constant Propagation for Explicitly Parallel Programs", 2nd HPCA Workshop on Interaction between Compilers and Computer Architectures, San Antonio, Texas, Feb. 1997.

PUBLICATIONS

Refereed Journal Articles

[1] Yan Solihin, Jaejin Lee, and Josep Torrellas. "Automatic Code Mapping on an Intelligent Memory Architecture", *An extended version of [9], IEEE Transactions on Computers: Special Issue on Advances in High Performance Memory Systems*, Vol. 50, No 11, pp. 1248–1266, Nov. 2001.

[2] Jaejin Lee and David A. Padua. "Hiding Relaxed Memory Consistency with a Compiler", *An extended version of [11], IEEE Transactions on Computers: Special Issue on Parallel Architectures and Compilation Techniques*, Vol. 50, No 8, pp. 824–833, Aug. 2001.

[3] Jaejin Lee, Samuel P. Midkiff, and David A. Padua. "A Constant Propagation Algorithm for Explicitly Parallel Programs", *International Journal of Parallel Programming*, Vol. 26, No 5, pp. 563–589, Dec. 1998.

[4] William Blume, Ramon Doallo, Rudolf Eigenmann, John Grout, Jay Hoeflinger, Thomas Lawrence, Jaejin Lee, David Padua, Yunheung Paek, Bill Pottenger, Lawrence Rauchwerger, and Peng Tu. "Parallel Programming with Polaris", *IEEE Computer*, Vol. 29, No. 12, pp. 78–82, Dec. 1996.

Refereed Conference and Workshop Papers

[5] Yan Solihin, Jaejin Lee, and Josep Torrellas. "Memory-Side Correlation Prefetching Using a General-Purpose Core in Memory" To appear in the 29th Annual International Symposium on Computer Architecture (ISCA 2002), Anchorage, Alaska, May 2002.

[6] Yan Solihin, Jaejin Lee, and Josep Torrellas. "Prefetching in an Intelligent Memory Architecture Using a Helper Thread", *Proceedings of the 5th Workshop on Multithreaded Execution, Architecture and Compilation (MTEAC-5, in conjunction with MICRO-34)*, Dec. 2001. (Best paper award)

[7] Betty Cheng, Laura Dillon, Kurt Stirewalt, Philip McKinley, Sadeep Kulkarni, and Jaejin Lee. "Automated Development and Run-time Adaptation of Interactive Distributed Applications", *NSF Workshop on New Visions for Software Design and Productivity: Research and Applications (Software Design and Productivity Coordinating Group, http://www.isis.vanderbilt.edu/sdp/Papers/Papers.htm)*, Dec. 2001.

[8] Samuel P. Midkiff, Jaejin Lee, David A. Padua. "A Compiler for Multiple Memory Models", *Proceedings of the 9th Workshop on Compilers for Parallel Computers (CPC 2001, http://www.icsa.informatics.ed.ac.uk/cpc2001/)*, Edinburgh, Scotland, UK, Jun. 2001

[9] Jaejin Lee, Yan Solihin, and Josep Torrellas. "Automatically Mapping Code on an Intelligent Memory Architecture", *Proceedings of the 7th International Symposium on High Performance Computer Architecture (HPCA-7)*, Monterrey, Mexico, Jan. 2001.

[10] Yan Solihin, Jaejin Lee, and Josep Torrellas. "Adaptively Mapping Code in an Intelligent Memory Architecture", *Proceedings of the 2nd Workshop on Intelligent Memory Systems (IMS 2000, in conjunction with ASPLOS-IX), Lecture Notes in Computer Science 2107, Springer*, Cambridge, Massachusetts, pp. 71–84, Nov. 2000.

[11] Jaejin Lee and David A. Padua. Hiding Relaxed Memory Consistency with Compilers. *Proceedings of the 2000 International Conference on Parallel Architectures and Compilation Techniques (PACT)*, Philadelphia, Pensilvania, pp. 111–122, Oct. 2000.

[12] Jaejin Lee, David A. Padua, and Samuel P. Midkiff. "Basic Compiler Algorithms for Parallel Programs", *Proceedings of the 7th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP)*, Atlanta, Georgia, pp. 1–12, May 1999.

[13] Jaejin Lee, Samuel P. Midkiff, and David A. Padua. "Concurrent Static Single Assignment Form and Constant Propagation for Explicitly Parallel Programs", *Proceedings of the 10th International Workshop on Languages and Compilers for Parallel Computing (LCPC), Lecture Notes in Computer Science 1366, Springer*, pp. 114–130, Twin Cities, Minnesota, Aug. 1997.

[14] Jaejin Lee and David A. Padua. "Parallel Static Single Assignment Form and Constant Propagation for Explicitly Parallel Programs", *Proceedings of the 2nd HPCA Workshop on Interaction between Compilers and Computer Architectures*, San Antonio, Texas, Feb. 1997.

[15] William Blume, Rudolf Eigenman, K. Faigin, John Grout, Thomas Lawrence, Jaejin Lee, Jay Hoeflinger, David Padua, Yunheung Paek, Paul Petersen, William Pottenger, Lawrence Rauchwerger, Stephen Weatherford, and Peng Tu. "Restructuring Programs for High-Speed Computers with Polaris", *Proceedings of the 1996 ICPP Workshop on Challenges for Parallel Processing*, Aug. 1996.

[16] Zohar Manna, Nikolaj Bjórner, Anca Browne, Edward Chang, Michael Colon, Luca de Alfaro, Harish Devarajan, Arjun Kapur, Jaejin Lee, Henny Sipma, and Tomas E. Uribe. "STeP: The Stanford Temporal Prover", *TAPSOFT'95: Theory and Practice of Software Development, 6th International Joint Conference CAAP/FASE, Lecture Notes in Computer Science 915, Springer*, pp. 793–794, May 1995.

Technical Reports

[17] Jaejin Lee and David A. Padua. "A Compiler Technique to Hide Relaxed Memory Consistency", *Technical Report MSU-CSE-01-13*, Department of Computer Science and Engineering, Michigan State University, Apr. 2001.

[18] Jaejin Lee, David A. Padua, and Samuel P. Midkiff. "Basic Compilation Techniques for Explicitly Parallel Programs", *Technical Report MSU-CSE-01-14*, Department of Computer Science and Engineering, Michigan State University, Apr. 2001.

[19] Jaejin Lee, "Hiding the Java Memory Model with Compilers", *Technical Report MSU-CSE-00-29*, Department of Computer Science and Engineering, Michigan State University, Dec. 2000.

[20] Jaejin Lee, "Compilation Techniques for Explicitly Parallel Programs", *Ph.D. Thesis, Technical Report UIUCDCS-R-99-2112*, Department of Computer Science, University of Illinois at Urbana-Champaign, Oct. 1999.

[21] Jaejin Lee, Samuel P. Midkiff, and David A. Padua, "Concurrent Static Single Assignment Form and Concurrent Sparse Conditional Constant Propagation for Explicitly Parallel Programs", *Technical Report TR#1525*, CSRD, University of Illinois at Urbana-Champaign, Jul. 1997.

[22] William Blume, Rudolf Eigenman, K. Faigin, John Grout, Thomas Lawrence, Jaejin Lee, Jay Hoeflinger David Padua, Yunheung Paek, Paul Petersen, William Pottenger, Lawrence Rauchwerger, S. Weatherford, and Peng Tu. "Advanced program restructuring for high-performance computers with Polaris", *Technical Report TR#1473*, CSRD, University of Illinois at Urbana-Champaign, Jan. 1996.

In Preparation

[23]Jaejin Lee, David A. Padua, and Samuel P. Midkiff. "Basic Compiler Algorithms for Explicitly Parallel Programs", *An extended version of [12]*, Accepted with revision, ACM Transactions on Programming Languages and Systems, Jun. 2001.

[24] Samuel P. Midkiff, Jaejin Lee, David A. Padua, "A Compiler for Multiple Memory Models", Submitted for publication.