Milestone #10

Milestone Overview

You will augment your pipelined MIPSlite microprocessor so that it correctly handles control hazards.

This project milestone is worth 40 points. For full credit, your solution must be completed no later than Thursday, April 20. A 10% penalty will be applied for each day that your solution is late (based on the date when your files are submitted via the "handin" system).

Milestone Deliverables

The deliverables for this milestone are:

DataHazardUnit.c
MemoryUnit.c
BranchUnit.c
machine.c

Be sure to use the specified file names, and to submit your files for grading via the "handin" system.

Milestone Specifications

Control transfer instructions are currently processed in the third pipeline stage, which means that there are two delay slots following each transfer of control.

For this milestone, you will move the Branch Unit to the second stage of your pipelined machine from Milestone #9 in order to eliminate the second delay slot. There will still be one delay slot following each transfer of control: the instruction immediately following a control transfer instruction will always be fetched and executed.

Create a new project subdirectory under your account and copy the appropriate files, including your "MemoryUnit.c", "BranchUnit.c" and "machine.c", as well as the following instructor-supplied files:

/user/cse420/Project/Milestone10/machine*

The following instructor-supplied files are available but must not be copied into your account:

/user/cse420/Project/Milestone10/ClockUnit*
/user/cse420/Project/Milestone10/FetchUnit*
/user/cse420/Project/Milestone10/ControlUnit*
/user/cse420/Project/Milestone10/RegisterUnit*
/user/cse420/Project/Milestone10/DisplayUnit*
/user/cse420/Project/Milestone10/ShiftUnit*
/user/cse420/Project/Milestone10/MathUnit*
/user/cse420/Project/Milestone10/BranchUnit.h
/user/cse420/Project/Milestone10/MemoryUnit.h
/user/cse420/Project/Milestone10/DataHazardUnit.h

The ten components behave as specified in the previous milestones.
The following diagram gives the structure of a pipelined implementation of the MIPSlite microprocessor.

The inputs to the Branch Unit remain as before. However, those signals will now come from the second stage of the pipeline and the 1-bit zero flag will be generated using a "Compare" component (instead of being generated by the Math Unit in the third stage).

The 32-bit return address will be captured in the ID/EX pipeline register and then available in the third stage of the pipeline during the next clock cycle.