As you prepare for Exam #2, I would suggest that you review your lecture notes and the readings in the Patterson and Hennessy textbook for the main topics that we covered since Exam #1:

- Pipelined Processors (P&H, 4.5-4.10)
- The Memory Hierarchy (P&H, 5.1-5.11)

Some suggestions about questions that might appear on the exam:

a) Given a MIPS machine language instruction, give the value of each signal for a specified datapath (for example, the datapath shown in Figure 4.51).

b) Given a specified datapath, discuss the impact of data hazards.

c) Given a specified datapath, discuss the impact of control hazards.

d) Given a specified cache system, indicate how read and write requests are handled.

e) Given a specified virtual memory system, indicate how memory references are handled.

I have included several sample questions at the end of this file. You might want to work those questions and even create new questions by substituting different machine language instructions and/or data values.

You might also consider reviewing some of the exercises at the end of each textbook chapter.

--M. McCullen
1. Consider the pipelined MIPS datapath in Figure 4.65 and the instruction sequence shown below. In the spaces provided, give the name of the pipeline register (such as "IF/ID") from which the indicated operands are routed to the ALU.

```
addi $2, $0, 0x7800
addi $3, $0, 0x3400
add $4, $3, $2 $3: ____________ $2: ____________
ori $5, $3, 40 $3: ____________ 40: ____________
sub $6, $2, $5 $2: ____________ $5: ____________
```

2. Consider the pipelined MIPS datapath in Figure 4.65 and the instruction sequence shown below. In the spaces provided, give the name of the pipeline register (such as "IF/ID") from which the indicated operands are routed to the ALU.

```
addi $2, $0, 0x3200
addi $3, $0, 0x6700
sub $4, $2, $3 $2: ____________ $3: ____________
lw $5, 80 ($4) $4: ____________ 80: ____________
add $6, $4, $5 $4: ____________ $5: ____________
```
3. Consider the pipelined MIPS datapath in Figure 4.51 and the register contents (in hexadecimal) shown below. The fields within the IF/ID pipeline register at time T+0 are shown below in hexadecimal, with explanatory comments. You may assume that there are no data hazards.

IF/ID.nextPC: 0000503c (value of PC register incremented by 4)
IF/ID.instruction: 8c448800 (equivalent to "lw $4, 0x8800 ($2)"

For each of the pipeline register fields listed below, give the contents of the field (in hexadecimal) at the specified time. If the value of a particular field cannot be determined, write "Unknown".

Register File:

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R00</td>
<td>00000000</td>
</tr>
<tr>
<td>R01</td>
<td>ffffffff</td>
</tr>
<tr>
<td>R02</td>
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</tr>
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<td>00000017</td>
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<td>0000000f</td>
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<td>ff33e5c0</td>
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<tr>
<td>R12</td>
<td>0000012</td>
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<tr>
<td>R13</td>
<td>0000001d</td>
</tr>
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<td>R14</td>
<td>000004c6</td>
</tr>
<tr>
<td>R15</td>
<td>0000098c</td>
</tr>
<tr>
<td>R16</td>
<td>ff29bbd0</td>
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<tr>
<td>R17</td>
<td>0000002f</td>
</tr>
<tr>
<td>R18</td>
<td>00021258</td>
</tr>
<tr>
<td>R19</td>
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<td>R20</td>
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<tr>
<td>R30</td>
<td>00021260</td>
</tr>
<tr>
<td>R31</td>
<td>00021264</td>
</tr>
</tbody>
</table>

a) ID/EX pipeline register at time T+1

ID/EX.RegDst: ____________ ID/EX.ALUSrc: ____________
ID/EX.ReadData1: ________________________
ID/EX.ReadData2: ________________________
ID/EX.immediate: ________________________
ID/EX.rt: ____________
ID/EX.rd: ____________

b) EX/MEM pipeline register at time T+2

EX/MEM.MemRead: ____________ EX/MEM.MemWrite: ____________
EX/MEM.ALUresult: ________________________
EX/MEM.ReadData2: ________________________
EX/MEM.rd: ____________

c) MEM/WB pipeline register at time T+3

MEM/WB.MemToReg: ____________ MEM/WB.RegWrite: ____________
MEM/WB.ReadData: ________________________
MEM/WB.ALUresult: ________________________
MEM/WB.rd: ____________
4. Consider the pipelined MIPS datapath in Figure 4.51. Answer each question clearly but concisely.

a) What is the purpose of the component labeled "Add" in the third stage of the pipeline? Explain completely but concisely.

b) If the processor uses "assume branch not taken", what is the branch penalty (in clock cycles) when a branch is taken? Explain completely but concisely.

5. Consider the pipelined MIPS datapath in Figure 4.65. Answer each question clearly but concisely.

a) If the processor uses "assume branch not taken", what is the branch penalty (in clock cycles) when a branch is taken? Explain completely but concisely.

b) Some processors have an explicit "delay slot" to allow a useful instruction to be executed immediately after a branch instruction. Does the datapath in Figure 4.65 have an explicit delay slot? Explain completely but concisely.
6. Consider the following characteristics for the components in a memory hierarchy, where the stated access times include all miss processing for higher levels of the hierarchy.

   One access to Level 1 cache consumes 2 nanoseconds
   One access to Level 2 cache consumes 10 nanoseconds
   One access to primary storage (RAM) consumes 40 nanoseconds

If 90% of memory references result in a hit in level 1 cache, 80% of the remaining references result in a hit in Level 2 cache, and all others are satisfied from RAM, what is the average memory access time?

7. The instruction cache for an implementation of the MIPS is a direct-mapped cache which contains 8192 slots. The control bits for each slot are a valid bit and a modified bit. A cache line is 4 bytes.

   a) How is a 32-bit address viewed by this cache organization?

   b) What is the total number of bits in one cache slot?

8. A byte-oriented virtual memory system has the following characteristics.

   Virtual address: 32 bits
   Physical address: 36 bits
   Size of one page: 4 kilobytes

The TLB is fully associative and contains 128 slots. Each slot has three control bits (a valid bit, a referenced bit, and a modified bit).

   a) How is a 32-bit virtual address viewed by this memory system?

   b) Assuming the system uses a one-level page table, what is the maximum size of the page table?

   c) How many bits does one TLB slot contain?
The data cache for an implementation of the MIPS is a direct-mapped, write-back, write-allocate cache which contains 16 slots. The control bits for each slot are a valid bit and a modified bit. A cache line is 16 bytes.

The current cache entries are shown below (in hexadecimal). For clarity, the 16-byte data blocks are not shown.

<table>
<thead>
<tr>
<th>Index</th>
<th>Valid</th>
<th>Dirty</th>
<th>Tag bits</th>
<th>Index</th>
<th>Valid</th>
<th>Dirty</th>
<th>Tag bits</th>
</tr>
</thead>
<tbody>
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<td>0</td>
<td>FFF641</td>
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<td>0</td>
<td>0</td>
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<td>9</td>
<td>1</td>
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<td>000014</td>
<td>F</td>
<td>1</td>
<td>1</td>
<td>00003A</td>
</tr>
</tbody>
</table>

a) What are the first and last addresses of the bytes stored in the data field at index 9?

b) Assume that the current program sends the address FF987654 (hexadecimal) to the data cache. To which cache slot is that address mapped?

c) Assume that the current program executes a "LW" instruction, which results in a "miss" in the data cache. What steps are taken to process the miss?

d) Assume that the current program executes a "SW" instruction, which results in a "hit" in the data cache. What steps are taken to process the hit?
1. Consider the pipelined MIPS datapath in Figure 4.65 and the instruction sequence shown below. In the spaces provided, give the name of the pipeline register (such as "IF/ID") from which the indicated operands are routed to the ALU.

   addi $2, $0, 0x7800
   addi $3, $0, 0x3400
   add $4, $3, $2       $3:  __EX/MEM__________    $2:  __MEM/WB__________
   ori $5, $3, 40       $3:  __MEM/WB__________    40:  __ID/EX___________
   sub $6, $2, $5       $2:  __ID/EX___________    $5:  __EX/MEM__________

2. Consider the pipelined MIPS datapath in Figure 4.65 and the instruction sequence shown below. In the spaces provided, give the name of the pipeline register (such as "IF/ID") from which the indicated operands are routed to the ALU.

   addi $2, $0, 0x3200
   addi $3, $0, 0x6700
   sub $4, $2, $3       $2:  __MEM/WB__________    $3:  __EX/MEM__________
   lw $5, 80 ($4)       $4:  __EX/MEM__________    80:  __ID/EX___________
   add $6, $4, $5       $4:  __ID/EX___________    $5:  __MEM/WB__________
3. Consider the pipelined MIPS datapath in Figure 4.51 and the register contents (in hexadecimal) shown below. The fields within the IF/ID pipeline register at time T+0 are shown below in hexadecimal, with explanatory comments. You may assume that there are no data hazards.

IF/ID.nextPC: 0000503c (value of PC register incremented by 4)
IF/ID.instruction: 8c448800 (equivalent to "$4, 0x8800 ($2)"

For each of the pipeline register fields listed below, give the contents of the field (in hexadecimal) at the specified time. If the value of a particular field cannot be determined, write "Unknown".

Register File:
R00: 00000000 R08: 00021258 R10: 0000000f R18: 00021258
R01: ffffffff R09: 0002126c R11: 00000017 R19: 0002125c
R02: 00020a50 R0A: ff33e5c0 R12: 00000012 R1A: 00021260
R03: 00444440 R0B: 00000300 R13: 0000001d R1B: 00021264
R04: 00010855 R0C: 00022768 R14: 000004c6 R1C: 00021268
R05: 00000000 R0D: ff29bbd0 R15: 0000098c R1D: 00000000
R06: 00010a10 R0E: ffbef900 R16: 0000002f R1E: ffbef960
R07: 000100ff R0F: 000107c8 R17: 00000034 R1F: 000105d4

a) ID/EX pipeline register at time T+1
ID/EX.RegDst: __0_________  ID/EX.ALUSrc: __1_________
ID/EX.ReadData1: __00020A50______________
ID/EX.ReadData2: __00010855______________
ID/EX.immediate: __FFFF8800______________
ID/EX.rt: __04_______
ID/EX.rd: __11________

b) EX/MEM pipeline register at time T+2
EX/MEM.MemRead: __1_________  EX/MEM.MemWrite: __0_________
EX/MEM.ALUresult: __00019250______________
EX/MEM.ReadData2: __00010855______________
EX/MEM.rd: __04_______

c) MEM/WB pipeline register at time T+3
MEM/WB.MemToReg: __1_________  MEM/WB.RegWrite: __1_________
MEM/WB.ReadData: __unknown______________
MEM/WB.ALUresult: __00019250______________
MEM/WB.rd: __04_______
4. Consider the pipelined MIPS datapath in Figure 4.51. Answer each question clearly but concisely.

a) What is the purpose of the component labeled "Add" in the third stage of the pipeline? Explain completely but concisely.

The "Add" component computes the target address for branch instructions:

\[(PC+4) + \text{sign\_ext\( (\text{simm16}) |00\)}\]

b) If the processor uses "assume branch not taken", what is the branch penalty (in clock cycles) when a branch is taken? Explain completely but concisely.

The branch penalty is 3 clock cycles, since the next three instructions following the branch have been fetched into the pipeline before the branch is resolved in the 4th stage.

5. Consider the pipelined MIPS datapath in Figure 4.65. Answer each question clearly but concisely.

a) If the processor uses "assume branch not taken", what is the branch penalty (in clock cycles) when a branch is taken? Explain completely but concisely.

The branch penalty is one clock cycle, since the next instruction following the branch has been fetched into the pipeline before the branch is resolved in the 2nd stage.

b) Some processors have an explicit "delay slot" to allow a useful instruction to be executed immediately after a branch instruction. Does the datapath in Figure 4.65 have an explicit delay slot? Explain completely but concisely.

No, there is no delay slot in Figure 4.65. If the branch is taken, the instruction following the branch is flushed from the pipeline using the "IF.Flush" control signal.
6. Consider the following characteristics for the components in a memory hierarchy, where the stated access times include all miss processing for higher levels of the hierarchy.

One access to Level 1 cache consumes 2 nanoseconds
One access to Level 2 cache consumes 10 nanoseconds
One access to primary storage (RAM) consumes 40 nanoseconds

If 90% of memory references result in a hit in level 1 cache, 80% of the remaining references result in a hit in Level 2 cache, and all others are satisfied from RAM, what is the average memory access time?

\[
AMAT = 2.0 \text{ ns} + 0.10 \times 10 \text{ ns} + 0.02 \times 40 \text{ ns} \\
= 3.8 \text{ ns}
\]

7. The instruction cache for an implementation of the MIPS is a direct-mapped cache which contains 8192 slots. The control bits for each slot are a valid bit and a modified bit. A cache line is 4 bytes.

a) How is a 32-bit address viewed by this cache organization?

- Tag -- 17 bits
- Index -- 13 bits
- Byte offset -- 2 bits

b) What is the total number of bits in one cache slot?

51 bits (valid bit + modified bit + tag + data)

8. A byte-oriented virtual memory system has the following characteristics.

- Virtual address: 32 bits
- Physical address: 36 bits
- Size of one page: 4 kilobytes

The TLB is fully associative and contains 128 slots. Each slot has three control bits (a valid bit, a referenced bit, and a modified bit).

a) How is a 32-bit virtual address viewed by this memory system?

- Virtual page number -- 20 bits
- Page offset -- 12 bits

b) Assuming the system uses a one-level page table, what is the maximum size of the page table?

\(2^{20} \text{ entries} \ (1,048,576 \text{ entries})\)

c) How many bits does one TLB slot contain?

47 bits (3 control bits + virtual page number + physical page number)
9. The data cache for an implementation of the MIPS is a direct-mapped, write-back, write-allocate cache which contains 16 slots. The control bits for each slot are a valid bit and a modified bit. A cache line is 16 bytes.

The current cache entries are shown below (in hexadecimal). For clarity, the 16-byte data blocks are not shown.

<table>
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<tr>
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<th>Valid</th>
<th>Dirty</th>
<th>Tag bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>FFF641</td>
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<td>1</td>
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<table>
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</tr>
<tr>
<td>F</td>
<td>1</td>
<td>1</td>
<td>00003A</td>
</tr>
</tbody>
</table>

a) What are the first and last addresses of the bytes stored in the data field at index 9?

Addresses 00002890 and 0000289F (hexadecimal)

b) Assume that the current program sends the address FF987654 (hexadecimal) to the data cache. To which cache slot is that address mapped?

Cache slot 5

c) Assume that the current program executes a "LW" instruction, which results in a "miss" in the data cache. What steps are taken to process the miss?

Sixteen bytes were copied from the RAM to the data cache.
The valid bit was set to 1.
The dirty bit was set to 0.

d) Assume that the current program executes a "SW" instruction, which results in a "hit" in the data cache. What steps are taken to process the hit?

The dirty bit was set to 1.