Lab Exercise #6 Solution

1. Consider the following characteristics for components in a memory system:

   A successful access to Level 1 cache consumes 2 nanoseconds
   A successful access to Level 2 cache consumes 10 nanoseconds
   A successful access to primary storage (RAM) consumes 40 nanoseconds

Assume that the stated access times include all miss processing for higher levels of the hierarchy.

a) A given system contains Level 1 cache and primary storage, but no Level 2 cache. If 90% of memory references result in a hit in level 1 cache and all other references are satisfied from primary storage, what is the average memory access time?

   AMAT = 1.00 * 2 ns + 0.10 * 40 ns = 6.0 ns

b) A given system contains Level 1 cache, Level 2 cache, and primary storage. If 90% of memory references result in a hit in level 1 cache, 80% of the remaining references result in a hit in Level 2 cache, and all other references are satisfied from primary storage, what is the average memory access time?

   AMAT = 1.00 * 2 ns + 0.10 * 10 ns + 0.02 * 40 ns = 3.8 ns

c) A given system contains Level 1 cache, Level 2 cache, and primary storage. If 95% of memory references result in a hit in level 1 cache, 80% of the remaining references result in a hit in Level 2 cache, and all other references are satisfied from primary storage, what is the average memory access time?

   AMAT = 1.00 * 2 ns + 0.05 * 10 ns + 0.01 * 40 ns = 2.9 ns
2. Consider a byte-oriented memory system with 4-byte words and 32-bit physical addresses. Assume that the cache is direct mapped and has 16 blocks, with 4 words per block. The current cache entries are shown below in hexadecimal; for clarity, the 4-word blocks are not shown.

<table>
<thead>
<tr>
<th>Index</th>
<th>Valid</th>
<th>Dirty</th>
<th>Tag bits</th>
<th>Index</th>
<th>Valid</th>
<th>Dirty</th>
<th>Tag bits</th>
</tr>
</thead>
<tbody>
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Answer each of the following questions completely but concisely.

a) Give the size (in bits) of 1 cache entry, including all control and data bits.

\[
\text{one cache entry} = \text{valid} + \text{dirty} + \text{tag} + \text{data bits} \\
= 1 + 1 + 24 + 128 \text{ bits} \\
= 154 \text{ bits}
\]

b) Consider the cache entry at index B. What are the physical addresses of the first and last bytes currently contained in that cache entry?

first byte: FFFF7CB0
last byte: FFFF7CBF

c) Given the current entries in the cache, is it possible for a subsequent reference by the current process to cause a compulsory cache miss? Explain.

Yes. A compulsory miss is a cache miss caused by the first reference to an address in a given block. A process can refer to new addresses as long as it continues to execute.

The cache contains blocks referenced in the past and does not preclude the process referring to new addresses as it continues to execute.
3. Consider a byte-oriented memory system with 4-byte words and 32-bit physical addresses. Assume that the cache is direct mapped and has 16 blocks, with 4 words per block. The current cache cache entries are shown below in hexadecimal; for clarity, the 4-word blocks are not shown.

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For each of the following memory references, explain the steps used to process the reference. Include information such as whether it causes a cache hit or miss, any interaction with the next lower level of the memory hierarchy, and any changes to the cache entries.

a) The current process reads from physical address FFF59A8C (hexadecimal).

Examine entry 8 of cache
Miss -- valid bit is 0
Copy block containing address FFF59A8C from next lower level of memory hierarchy to entry 8 of cache
Set tag bits to FFF59A
Set valid bit to 1
Set dirty bit to 0
Satisfy read request using data block of entry 8

b) The current process writes to physical address 00003A28 (hexadecimal).

Examine entry 2 of the cache
Hit -- valid bit is 1 and tags match
Set dirty bit to 1
Satisfy write request using data block of entry 2

c) The current process reads from physical address 00002D40 (hexadecimal).

Examine entry 4 of the cache
Miss -- valid bit is 1 but tags do not match
Valid bit is 1 and dirty bit is 1, so copy data block to next lower level of memory hierarchy (addresses FFFF7C40 to FFFF7C4F)
Copy block containing address 00002D40 from next lower level of memory hierarchy to entry 4 of cache
Set tag bits to 00002D
Set valid bit to 1
Set dirty bit to 0
Satisfy read request using data block of entry 4
4. Consider a byte-oriented memory system with 4-byte words and 32-bit physical addresses. Assume that the cache has 16 words per block, and has 128 kilobytes of storage for blocks. Give the number of bits in one tag and one index for each of the cache organizations below.

a) Direct-mapped cache
   Bits in 1 tag: __15_____
   Bits in 1 index: __11_____

b) Fully associative cache
   Bits in 1 tag: __26_____
   Bits in 1 index: __0_____