Exam #2 Study Suggestions

Major Areas

Memory Management
Virtual Memory

Materials

Lecture notes from 10/5 through 11/2
Chapter 1 (pages 21-25, 33-39) of the Stallings text
Chapter 7 of the Stallings text
Chapter 8 of the Stallings text
Self-study Exercise #6
Self-study Exercise #7
Self-study Exercise #8

Topics

The memory hierarchy
Locality of reference (temporal and spatial)
Average memory access time (AMAT)
Cache memory
Cache organizations (direct mapped, fully associative)
Main memory
Fixed and dynamic partitioning
Simple paging
Simple segmentation
Virtual memory
Paging within a virtual memory system
Hardware support
Page fault processing
Fetch policies
Replacement policies
Page buffering
Resident set management
Cleaning policy
Load control
Multi-level page tables
Virtual memory in Linux systems

Review Questions

1. In your own words, define the term “locality of reference”.
2. In your own words, define the term “temporal locality”.
3. In your own words, define the term “spatial locality”.
4. In your own words, define the term “virtual memory”. 
5. Consider the following characteristics for the components in a memory hierarchy, where the stated access times include all miss processing for higher levels of the hierarchy.

   A successful access to Level 1 cache consumes 1 nanosecond
   A successful access to primary storage (RAM) consumes 50 nanoseconds

If 95% of memory references result in a hit in level 1 cache, and all others are satisfied from RAM, what is the average memory access time?

   A) 2.5 ns
   B) 3.5 ns
   C) 5.0 ns
   D) 6.0 ns
   E) None of the above.

6. Consider the following characteristics for the components in a memory hierarchy, where the stated access times include all miss processing for higher levels of the hierarchy.

   A successful access to Level 1 cache consumes 1 nanosecond
   A successful access to Level 2 cache consumes 10 nanoseconds
   A successful access to primary storage (RAM) consumes 50 nanoseconds

If 90% of memory references result in a hit in level 1 cache, 90% of the remaining references result in a hit in Level 2 cache, and all others are satisfied from RAM, what is the average memory access time?

   A) 1.5 ns
   B) 2.0 ns
   C) 2.5 ns
   D) 3.0 ns
   E) None of the above.

7. Consider the instruction cache described in Figure 1. What is the total number of bits in one cache slot?

   A) 47 bits
   B) 49 bits
   C) 51 bits
   D) 53 bits
   E) None of the above.

8. Consider the instruction cache described in Figure 1. Which of the following statements about that cache organization is correct?

   A) It exploits temporal locality, but not spatial locality.
   B) It requires two 30-bit comparators per slot.
   C) It exploits spatial locality, but not temporal locality.
   D) It requires four 30-bit comparators per slot.
   E) It exploits both temporal locality and spatial locality.
A microprocessor has 32-bit physical addresses. The data cache is a direct-mapped, write-back cache with 16 slots. The control bits for each slot are a valid bit (V) and a modified bit (M). A cache block is 256 bytes.

The current cache entries are shown below (in hexadecimal). For clarity, the 256-byte data blocks are not shown.

<table>
<thead>
<tr>
<th>Index</th>
<th>V</th>
<th>M</th>
<th>Tag</th>
<th>Index</th>
<th>V</th>
<th>M</th>
<th>Tag</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>FF641</td>
<td>8</td>
<td>0</td>
<td>0</td>
<td>0004A</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>00014</td>
<td>9</td>
<td>1</td>
<td>0</td>
<td>00028</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>0003A</td>
<td>A</td>
<td>1</td>
<td>0</td>
<td>00028</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>FF593</td>
<td>B</td>
<td>1</td>
<td>1</td>
<td>FFF7C</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>1</td>
<td>FFF7C</td>
<td>C</td>
<td>0</td>
<td>1</td>
<td>00EA1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
<td>00014</td>
<td>D</td>
<td>1</td>
<td>0</td>
<td>00028</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>0</td>
<td>00014</td>
<td>E</td>
<td>1</td>
<td>1</td>
<td>0003A</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>0</td>
<td>00014</td>
<td>F</td>
<td>1</td>
<td>1</td>
<td>0003A</td>
</tr>
</tbody>
</table>

9. Consider the information in Figure 2. What are the first and last addresses of the bytes stored in the data field at index 9?

A) 00000028 and 00000037 (hexadecimal)
B) 00000280 and 0000028F (hexadecimal)
C) 00028900 and 000289FF (hexadecimal)
D) 00002890 and 0000289F (hexadecimal)
E) None of the above.

10. Consider the information in Figure 2. Assume that the current program sends the address FF987654 (hexadecimal) to the data cache. To which cache slot is that address mapped?

A) Slot 4
B) Slot 5
C) Slot 6
D) Slot F
E) None of the above.

11. Consider the information in Figure 2. Assume that the current program executes a "Load" instruction, which results in a "miss" in the data cache. Which of the following statements about the cache processing is correct?

A) 256 bytes were copied from the RAM to the data cache.
B) A modified bit was set to 1.
C) 256 bytes were copied from the data cache to the RAM.
D) A valid bit was set to 0.
E) None of the above.

12. Consider the information in Figure 2. Assume that the current program executes a "Store" instruction, which results in a "hit" in the data cache. Which of the following statements about the cache processing is correct?

A) 256 bytes were copied from the RAM to the data cache.
B) A modified bit was set to 1.
C) 256 bytes were copied from the data cache to the RAM.
D) A valid bit was set to 0.
E) None of the above.
A virtual memory system has the following characteristics:

- 15-bit virtual addresses
- 24-bit physical addresses
- 12-bit page offsets

The system does not have a TLB and uses demand paging.

The page table for the current process is shown below. Each page table entry has three control bits (valid (V), referenced (R) and modified (M)) and three access bits (read (r), write (w) and execute (x)). Page and frame numbers are given in hexadecimal, and all other items are given in binary.

<table>
<thead>
<tr>
<th>Page</th>
<th>V</th>
<th>RM</th>
<th>rwx</th>
<th>Frame</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>00</td>
<td>000</td>
<td>096</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>10</td>
<td>101</td>
<td>070</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>11</td>
<td>110</td>
<td>071</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>00</td>
<td>000</td>
<td>E42</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>11</td>
<td>110</td>
<td>074</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>00</td>
<td>000</td>
<td>B7C</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>00</td>
<td>000</td>
<td>065</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>10</td>
<td>110</td>
<td>073</td>
</tr>
</tbody>
</table>

The current process has a fixed allocation of five page frames (the frames numbered 70, 71, 72, 73 and 74 in hexadecimal).

13. Consider the information in Figure 3. Assume that the current program executes a "Load" instruction which references virtual address 72A4. Which of the following statements is correct?

   A) The instruction caused a page fault.
   B) The virtual address was mapped to the physical address 0732A4.
   C) The M bit of the page table entry was set to 1.
   D) All of the above.
   E) None of the above.

14. Consider the information in Figure 3. Assume that the current program executes a "Store" instruction which references virtual address 4C58. Which of the following statements is correct?

   A) The instruction did not cause a page fault.
   B) The virtual address was mapped to the physical address 074C58.
   C) The M bit of the page table entry was set to 1.
   D) All of the above.
   E) None of the above.

15. Consider the information in Figure 3. Assume that the current program executes a "Store" instruction which references virtual address 142C. Which of the following statements is correct?

   A) The instruction caused a page fault.
   B) The virtual address was mapped to the physical address 07042C.
   C) The M bit of the page table entry was set to 1.
   D) All of the above.
   E) None of the above.
A byte-oriented virtual memory system has the following characteristics.

Virtual address: 32 bits
Physical address: 36 bits
Size of one page: 4 kilobytes

The system uses a one-level page table. Each page table entry has three control bits (a valid bit, a referenced bit, and a modified bit) and three access bits (a read bit, a write bit, and an execute bit).

The TLB is fully associative and contains 128 slots.

16. Consider the information in Figure 4. How many page frames are present in the system?

A) $2^{12}$ frames (4,096 frames)
B) $2^{16}$ frames (65,536 frames)
C) $2^{20}$ frames (1,048,576 frames)
D) $2^{24}$ frames (16,777,216 frames)
E) None of the above.

17. Consider the information in Figure 4. How many page table entries are contained in the page table?

A) $2^{12}$ entries (4,096 entries)
B) $2^{16}$ entries (65,536 entries)
C) $2^{20}$ entries (1,048,576 entries)
D) $2^{24}$ entries (16,777,216 entries)
E) None of the above.

18. Consider the information in Figure 4. How many bits does one page table entry contain?

A) 26 bits
B) 30 bits
C) 44 bits
D) 50 bits
E) None of the above.

19. Consider the information in Figure 4. How many bits does one TLB slot contain?

A) 26 bits
B) 30 bits
C) 44 bits
D) 50 bits
E) None of the above.

20. Consider the information in Figure 4. Which of the following statements about that virtual memory system is correct?

A) It exploits temporal locality, but not spatial locality.
B) It requires one 12-bit comparator per TLB slot.
C) It exploits spatial locality, but not temporal locality.
D) It requires one 16-bit comparator per TLB slot.
E) It exploits both temporal locality and spatial locality.
A virtual memory system uses demand paging. A particular process has been given a fixed allocation of three pages frames and encounters the following sequence of page references: 3 4 0 4 1 3 4 3 1 0 1

For your convenience, a work area is provided at the bottom of this page.

21. Consider the information in Figure 5. What is the total number of page faults for the Optimal replacement algorithm?

A) 4 page faults, including 4 compulsory page faults.
B) 5 page faults, including 4 compulsory page faults.
C) 6 page faults, including 4 compulsory page faults.
D) 7 page faults, including 4 compulsory page faults.
E) None of the above.

22. Consider the information in Figure 5. What is the total number of page faults for the FIFO replacement algorithm?

A) 4 page faults, including 4 compulsory page faults.
B) 5 page faults, including 4 compulsory page faults.
C) 6 page faults, including 4 compulsory page faults.
D) 7 page faults, including 4 compulsory page faults.
E) None of the above.

23. Consider the information in Figure 5. What is the total number of page faults for the LRU replacement algorithm?

A) 4 page faults, including 4 compulsory page faults.
B) 5 page faults, including 4 compulsory page faults.
C) 6 page faults, including 4 compulsory page faults.
D) 7 page faults, including 4 compulsory page faults.
E) None of the above.

Work Area

```
frame 0
frame 1
frame 2

3 4 0 4 1 3 4 3 1 0 1
```

```
frame 0
frame 1
frame 2

3 4 0 4 1 3 4 3 1 0 1
```

```
frame 0
frame 1
frame 2

3 4 0 4 1 3 4 3 1 0 1
```
An operating system monitors the frequency with which page faults occur for a given process and adjusts the resources allocated to that process based on its page fault rate.

24. Consider the information in Figure 6. Which of the following statements about that operating system is correct?

A) When the page fault rate for a given process falls below the system's lower bound, the system deallocates a page frame from the process.
B) When the page fault rate for a given process rises above the system's upper bound, the system allocates a page frame to the process.
C) The system uses variable allocation and global replacement scope.
D) All of the above.
E) None of the above.

25. A virtual memory system uses a one-level page table and a fully associative TLB. Which of the following statements about that virtual memory system is correct?

A) When a particular page table entry is present in the TLB, that same page table entry will be present in the page table.
B) When a particular page table entry is present in the page table, that same page table entry will be present in the TLB.
C) When a particular page is present in RAM, the corresponding page table entry will be present in both the page table and the TLB.
D) All of the above.
E) None of the above.

Sample Exam Key (Multiple Choice Questions)