Directions:

a. DO NOT OPEN YOUR EXAM BOOKLET UNTIL YOU HAVE BEEN TOLD TO BEGIN.

b. This exam booklet contains 30 questions, each of which will be weighted equally. The exam is worth 180 points (18% of your course grade).

c. You may use one 8.5" x 11" note sheet (both sides) during the examination. No other reference materials or electronic devices (such as calculators) may be used during the examination.

d. You may not ask questions once the examination has begun.

If there is a structural problem with your exam booklet, such as a missing page or poorly printed page, please bring your exam booklet to the proctor.

If you believe that a question is ambiguous or contains a typographic error, write your interpretation of the question on the same page as the question, then put a note on the cover sheet of your exam booklet.

e. You should choose the single best alternative for each question, even if you believe that a question is ambiguous or contains a typographic error. If a question has more than one correct answer, full credit will be awarded for any correct answer.

f. Please fill in the requested information at the top of this exam booklet.

g. Use a #2 pencil to encode any information on your OMR form (bubble sheet).

h. Please encode the following on the OMR form:

   -- Last name and first initial
   -- MSU PID
   -- Exam form (2 X)

i. Only answers recorded on your OMR form will be counted for credit. Completely erase any responses on the OMR form that you wish to delete.

j. You must turn in this exam booklet and the OMR form when you have completed the exam. When leaving, please be courteous to those still taking the exam.
01. Consider two adjacent levels in a memory hierarchy, where all memory references are satisfied in one or the other of the two levels. Assume that access to the upper level consumes 3 nanoseconds, and that 95% of the memory references result in a hit in the upper level. If the average memory access time is 5 nanoseconds, what is the miss penalty?

A) 40 ns  
B) 60 ns  
C) 80 ns  
D) 100 ns  
E) None of the above.

02. Consider the following characteristics for the components in a memory hierarchy, where the stated access times include all miss processing for higher levels of the hierarchy.

Access to Level 1 cache consumes 1 nanosecond  
Access to primary storage (RAM) consumes 50 nanoseconds

If 97% of memory references result in a hit in level 1 cache, and all others are satisfied from RAM, what is the average memory access time?

A) 1.15 ns  
B) 1.5 ns  
C) 2.47 ns  
D) 2.5 ns  
E) None of the above.

03. Consider the following characteristics for the components in a memory hierarchy, where the stated access times include all miss processing for higher levels of the hierarchy.

Access to Level 1 cache consumes 1 nanosecond  
Access to primary storage (RAM) consumes 50 nanoseconds

What percentage of the accesses to cache must be a hit in order for the average memory access time to be 1.5 nanoseconds?

A) 90%  
B) 95%  
C) 97.5%  
D) 99%  
E) None of the above.

04. Consider the following characteristics for the components in a memory hierarchy, where the stated access times include all miss processing for higher levels of the hierarchy.

Access to Level 1 cache consumes 1 nanosecond  
Access to Level 2 cache consumes 20 nanoseconds  
Access to primary storage (RAM) consumes 50 nanoseconds

If 95% of the memory references result in a hit in level 1 cache, 90% of the remaining memory references result in a hit in Level 2 cache, and all other memory references are satisfied from RAM, what is the average memory access time?

A) 1.75 ns  
B) 2.0 ns  
C) 2.25 ns  
D) 4.5 ns  
E) None of the above.
05. Consider the instruction cache described in Figure 1. How large is the data block for one cache slot?

A) 8 bytes  
B) 16 bytes  
C) 32 bytes  
D) 64 bytes  
E) None of the above.

06. Consider the instruction cache described in Figure 1. Which of the following statements about that cache organization is correct?

A) The control bits for one cache slot include a Valid bit. 
B) The control bits for one cache slot include a Modified bit. 
C) The control bits for one cache slot include a Referenced bit. 
D) All of the above. 
E) None of the above.

07. Consider the instruction cache described in Figure 1. Which of the following statements about that cache organization is correct?

A) It exploits both temporal locality and spatial locality. 
B) It exploits temporal locality, but not spatial locality. 
C) It exploits spatial locality, but not temporal locality.  
D) It exploits neither temporal locality nor spatial locality.  
E) Locality of reference does not apply to instruction caches.

08. Consider the data cache described in Figure 2. How large is the tag for one cache slot?

A) 7 bits  
B) 19 bits  
C) 26 bits  
D) 32 bits  
E) None of the above.

09. Consider the data cache described in Figure 2. Which of the following statements about that cache organization is correct?

A) The control bits for one cache slot include a Valid bit.  
B) The control bits for one cache slot include a Modified bit. 
C) The data block for one cache slot contains 512 bits. 
D) All of the above. 
E) None of the above.
A microprocessor has 32-bit physical addresses. It has a direct-mapped write-back data cache with 16 slots and 16-byte blocks. The current cache contents are shown below (in hexadecimal).

<table>
<thead>
<tr>
<th>V M Tag</th>
<th>Block contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>[0]: 1 0 00020b 94 10 00 19 94 22 a0 01 40 00 43 1a 01 00 00 00</td>
<td></td>
</tr>
<tr>
<td>[1]: 1 1 7ebfda c4 1f bf 88 c8 1f bf 90 cc 1f bf 98 d0 1f bf a0</td>
<td></td>
</tr>
<tr>
<td>[2]: 1 1 00020c 01 00 00 00 80 8c a0 0f 12 80 00 07 01 00 00 00</td>
<td></td>
</tr>
<tr>
<td>[3]: 1 0 00020b e8 27 00 00 11 00 00 42 90 12 22 ec 13 00 00 43</td>
<td></td>
</tr>
<tr>
<td>[4]: 0 0 000000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00</td>
<td></td>
</tr>
<tr>
<td>[5]: 1 0 00020b 40 00 43 08 01 00 00 00 a4 04 a0 01 a2 04 60 01</td>
<td></td>
</tr>
<tr>
<td>[6]: 0 0 000000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00</td>
<td></td>
</tr>
<tr>
<td>[7]: 0 0 000000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00</td>
<td></td>
</tr>
<tr>
<td>[8]: 1 0 00020b 91 d0 20 23 d0 07 be fc 81 80 00 08 c1 1f bf 00</td>
<td></td>
</tr>
<tr>
<td>[9]: 1 1 00020c d9 3f bf 30 dd 3f bf 38 e1 3f bf 40 e5 3f bf 48</td>
<td></td>
</tr>
<tr>
<td>[a]: 1 0 7ebfda f9 3f bf 70 fd 3f bf 78 c0 3f bf 80 c4 3f bf 88</td>
<td></td>
</tr>
<tr>
<td>[b]: 1 1 7ebfda c8 3f bf 90 cc 3f bf 98 d0 3f bf a0 d4 3f bf a8</td>
<td></td>
</tr>
<tr>
<td>[c]: 1 0 000000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00</td>
<td></td>
</tr>
<tr>
<td>[d]: 0 0 000000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00</td>
<td></td>
</tr>
<tr>
<td>[e]: 0 0 000000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00</td>
<td></td>
</tr>
<tr>
<td>[f]: 1 1 00020b c1 2f be f0 11 00 00 43 90 12 20 fc 92 10 00 18</td>
<td></td>
</tr>
</tbody>
</table>

10. Consider the information in Figure 3. What are the first and last physical addresses of the bytes in the data block of slot 5 of the cache?

A) 0000020c and 0000021b (hexadecimal)
B) 000020c0 and 000020cf (hexadecimal)
C) 00020c00 and 00020cff (hexadecimal)
D) 40004308 and a2046001 (hexadecimal)
E) None of the above.

11. Consider the information in Figure 3. Assume that the current process sends the address 12345678 (hexadecimal) to the data cache. To which cache slot is that address mapped?

A) Slot 5
B) Slot 6
C) Slot 7
D) Slot 8
E) None of the above.

12. Consider the information in Figure 3. Assume that the current process executes a "Store" instruction where the target address is 11112222 hexadecimal. Which of the following statements about the processing of that instruction is correct?

A) 16 bytes were copied from slot 2 of the data cache to RAM.
B) The M bit in slot 2 was set to 1.
C) 16 bytes were copied from RAM to slot 2 of the data cache.
D) All of the above.
E) None of the above.
A microprocessor has 32-bit physical addresses. It has a direct-mapped write-back data cache with 16 slots and 16-byte blocks. The current cache contents are shown below (in hexadecimal).

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<tr>
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<td></td>
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<tr>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[3]: 1 0 00020b e8 27 00 00 11 00 00 42 90 12 22 ec 13 00 00 43</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[4]: 0 0 000000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[5]: 0 0 000000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[6]: 1 0 00020c 40 00 00 08 01 00 00 00 a4 04 a0 01 a2 04 01 00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[7]: 1 1 000088 91 d0 20 23 d0 07 be fc 81 80 00 08 c1 1f bf 00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[8]: 1 1 00020c d9 3f bf 30 dd 3f bf 38 e1 3f bf 40 e5 3f bf 48</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[a]: 0 0 000000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[b]: 1 0 7e6bda e9 3f bf 70 fd 3f bf 78 c0 3f bf 80 c4 3f bf 88</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[c]: 1 1 0000cc c8 3f bf 90 cc 3f bf 98 d0 3f bf a0 d4 3f bf a8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[d]: 0 0 000000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[e]: 0 0 000000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

13. Consider the information in Figure 4. Assume that the current process executes a "Load" instruction where the target address is 33334444 hexadecimal. Which of the following statements about the processing of that instruction is correct?

A) 16 bytes were copied from slot 4 of the data cache to RAM.
B) The M bit in slot 4 was set to 1.
C) 16 bytes were copied from RAM to slot 4 of the data cache.
D) All of the above.
E) None of the above.

14. Consider the information in Figure 4. Assume that the current process executes a "Store" instruction where the target address is 00008888 hexadecimal. Which of the following statements about the processing of that instruction is correct?

A) 16 bytes were copied from slot 8 of the data cache to RAM.
B) The M bit in slot 8 was set to 1.
C) 16 bytes were copied from RAM to slot 8 of the data cache.
D) All of the above.
E) None of the above.

15. Consider the information in Figure 4. Assume that the current process executes a "Load" instruction where the target address is 0000cccc hexadecimal. Which of the following statements about the processing of that instruction is correct?

A) 16 bytes were copied from slot c of the data cache to RAM.
B) The M bit in slot c was set to 1.
C) 16 bytes were copied from RAM to slot c of the data cache.
D) All of the above.
E) None of the above.
A byte-oriented virtual memory system which uses demand paging has the following characteristics.

Virtual address: 32 bits
Physical address: 40 bits
Size of one page: 8 kilobytes

The system uses a one-level page table. Each page table entry has three control bits (a valid bit, a referenced bit, and a modified bit) and three access bits (a read bit, a write bit, and an execute bit).

The TLB is fully associative and contains 256 slots.

16. Consider the information in Figure 5. How many page table entries are contained in the page table?
   A) $2^{13}$ entries (8,192 entries)
   B) $2^{19}$ entries (524,288 entries)
   C) $2^{20}$ entries (1,048,576 entries)
   D) $2^{27}$ entries (134,217,728 entries)
   E) None of the above.

17. Consider the information in Figure 5. How many bits does one page table entry contain?
   A) 25 bits
   B) 33 bits
   C) 38 bits
   D) 46 bits
   E) None of the above.

18. Consider the information in Figure 5. How many page frames are present in the system?
   A) $2^{13}$ frames (8,192 frames)
   B) $2^{19}$ frames (524,288 frames)
   C) $2^{20}$ frames (1,048,576 frames)
   D) $2^{27}$ frames (134,217,728 frames)
   E) None of the above.

19. Consider the information in Figure 5. How many bits does one TLB slot contain?
   A) 25 bits
   B) 33 bits
   C) 46 bits
   D) 52 bits
   E) None of the above.

20. Consider the information in Figure 5. Which of the following statements about the TLB in that virtual memory system is correct?
   A) The TLB exploits temporal locality, but not spatial locality.
   B) The TLB requires one 13-bit comparator per TLB slot.
   C) The TLB exploits spatial locality, but not temporal locality.
   D) The TLB requires one 27-bit comparator per TLB slot.
   E) The TLB exploits both temporal locality and spatial locality.
A byte-oriented virtual memory system which uses demand paging has the following characteristics:

- 16-bit virtual addresses
- 32-bit physical addresses
- 12-bit page offsets

The system does not have a TLB.

The page table for the current process is shown below. Each page table entry has three control bits (valid (V), referenced (R) and modified (M)) and three access bits ((read (r), write (w) and execute(x)). All values are given in hexadecimal or binary (for one-bit values).

<table>
<thead>
<tr>
<th>V</th>
<th>RM</th>
<th>rwx</th>
<th>Frame</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>--</td>
<td>---</td>
<td>-----</td>
</tr>
<tr>
<td>[0]: 1</td>
<td>11</td>
<td>110</td>
<td>00053</td>
</tr>
<tr>
<td>[1]: 0</td>
<td>10</td>
<td>101</td>
<td>00050</td>
</tr>
<tr>
<td>[2]: 1</td>
<td>11</td>
<td>110</td>
<td>00052</td>
</tr>
<tr>
<td>[3]: 0</td>
<td>10</td>
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<td>00054</td>
</tr>
<tr>
<td>[4]: 0</td>
<td>10</td>
<td>101</td>
<td>00054</td>
</tr>
<tr>
<td>[5]: 0</td>
<td>00</td>
<td>000</td>
<td>00000</td>
</tr>
<tr>
<td>[6]: 1</td>
<td>11</td>
<td>110</td>
<td>00050</td>
</tr>
<tr>
<td>[7]: 0</td>
<td>11</td>
<td>110</td>
<td>00051</td>
</tr>
</tbody>
</table>

The current process has a fixed allocation of five page frames: frames 50, 51, 52, 53 and 54 hexadecimal.

21. Consider the information in Figure 6. Assume that the current program executes a "Load" instruction which references virtual address 95a4. Which of the following statements about the processing of that reference is correct?

A) The system processed a page fault.
B) The virtual address was mapped to the physical address 000515a4.
C) The system set the V bit of page table entry 9 to 1.
D) All of the above.
E) None of the above.

22. Consider the information in Figure 6. Assume that the current program executes a "Store" instruction which references virtual address b7c8. Which of the following statements about the processing of that reference is correct?

A) The system copied 4096 bytes from RAM to disk.
B) The system copied 4096 bytes from disk to RAM.
C) The system set the M bit of page table entry b to 1.
D) All of the above.
E) None of the above.

23. Consider the information in Figure 6. Assume that the current program executes a "Load" instruction which references virtual address 3c60. Which of the following statements about the processing of that reference is correct?

A) The system copied 4096 bytes from RAM to disk.
B) The system copied 4096 bytes from disk to RAM.
C) The system set the M bit of page table entry 3 to 0.
D) All of the above.
E) None of the above.
A byte-oriented virtual memory system which uses demand paging has the following characteristics:

- 16-bit virtual addresses
- 32-bit physical addresses
- 12-bit page offsets

The system does not have a TLB.

The page table for the current process is shown below. Each page table entry has three control bits (valid (V), referenced (R) and modified (M)) and three access bits ((read (r), write (w) and execute(x)). All values are given in hexadecimal or binary (for one-bit values).

<table>
<thead>
<tr>
<th>Frame</th>
<th>V</th>
<th>RM</th>
<th>rwx</th>
<th>Frame</th>
<th>V</th>
<th>RM</th>
<th>rwx</th>
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<tbody>
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<td>110</td>
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<td>f</td>
<td>0</td>
<td>00</td>
</tr>
</tbody>
</table>

The current process has a fixed allocation of five page frames: frames 30, 31, 32, 33 and 34 hexadecimal.

24. Consider the information in Figure 7. Assume that the current program executes a "Store" instruction which references virtual address 6f20. Which of the following statements about the processing of that reference is correct?

A) The system processed a page fault.
B) The virtual address was mapped to the physical address 00031f20.
C) The system set the V bit of page table entry 6 to 1.
D) All of the above.
E) None of the above.

25. Consider the information in Figure 7. Assume that the current program executes a "Load" instruction which references virtual address 16a8. Which of the following statements about the processing of that reference is correct?

A) The system copied 4096 bytes from RAM to disk.
B) The system copied 4096 bytes from disk to RAM.
C) The system set the V bit of page table entry 1 to 1.
D) All of the above.
E) None of the above.

26. Consider the information in Figure 7. Assume that the current program executes a "Store" instruction which references virtual address 8a64. Which of the following statements about the processing of that reference is correct?

A) The system copied 4096 bytes from RAM to disk.
B) The system copied 4096 bytes from disk to RAM.
C) The system set the R bit of page table entry 8 to 1.
D) All of the above.
E) None of the above.
A byte-oriented virtual memory system uses a two-level page table. The top level of the page table is the Page Directory, where each entry in the Page Directory is 4 bytes wide. The second level of the page table consists of zero or more Page Maps, where each entry in a Page Map is 4 bytes wide.

The system has a page size of 1024 bytes, and there is no internal fragmentation in the pages which hold the page table.

27. Consider the information in Figure 8. Assuming that a virtual address consists of an index into the Page Directory, and index into a Page Map, and a page offset, what is the correct division of a virtual address into fields?

A) 8 bits, 8 bits, 10 bits
B) 8 bits, 9 bits, 10 bits
C) 9 bits, 8 bits, 10 bits
D) 9 bits, 9 bits, 10 bits
E) None of the above.

28. Consider the information in Figure 8. Assuming that the Page Directory contains 7 entries which are flagged as valid, how many pages are currently allocated to hold the page table?

A) 8 pages
B) 16 pages
C) 32 pages
D) 64 pages
E) None of the above.

29. Many microprocessors have a TLB (translation lookaside buffer). What is the main reason to have a TLB?

A) To allow the use of one-level page tables.
B) To allow the use of split instruction and data caches.
C) To allow the use of multi-level page tables.
D) To allow the use of multiple levels of cache.
E) None of the above.

30. A virtual memory system uses a one-level page table and a fully associative TLB. Which of the following statements about that system is correct?

A) When a particular page is present in RAM, the corresponding page table entry will be present in the TLB, but not necessarily in the page table.
B) When a particular page is present in RAM, the corresponding page table entry will be present in the page table, but not necessarily in the TLB.
C) When a particular page is present in RAM, the corresponding page table entry will always be present in both the page table and the TLB.
D) All of the above.
E) None of the above.