Lecture Topics

- Today: Microarchitecture
  (H&H 7.1-7.3)

Announcements

- Self-study Module #11
- Project #12 (due no later than 12/7)
Final Exam

- Thursday, 12/14 (12:45-2:45 PM)
- 24% of course grade
- 40 multiple choice questions
- Bring MSU ID, #2 pencils
- One 8.5x11 note sheet (both sides)

Patterson and Hennessey (2014):

Computers have led to a third revolution for civilization, with the information revolution taking its place alongside the agricultural and industrial revolutions.

This race to innovate has led to unprecedented progress since the inception of electronic computing in the late 1940s. Had the transportation industry kept pace with the computer industry, for example, today we could travel from New York to London in a second for a penny.
Moore’s Law

Observation in 1965: number of transistors on an integrated circuit doubles every 18-24 months (exponential growth).

A transistor’s dimensions are scaled by 30% every generation, so only 50% of the area is required (.7 x .7 = .49).

In other words, transistor density doubles.

Moore’s Law

Voltage used by a transistor is reduced by 30%, so power consumption is reduced by 50% (power based on voltage squared).

Also, signals only have to travel 70% as far, so clock speeds can increase by 40%.

Observation accurate for past 50 years.
Moore’s Law: Summary

Every 18-24 months:

- Transistor density doubles (each transistor only requires half the area)
- Power consumption remains the same (twice as many transistors, each requires only half the power)
- Circuits 40% faster (shorter distances)

Reducing program execution time

Improvements to the program:
- Better algorithms
- Better implementations

Improvements to the hardware:
- Faster clocks (and thus faster circuits)
- Parallelism
Parallelism

Instruction-level parallelism: overlap work at the level of individual instructions

- Pipelined processors
- Superscalar processors

Processor-level parallelism: overlap work at the level of the processor

- Multiple processors

Patterson’s laundry example

- Ann, Brian, Cathy, Dave each has one load of clothes to wash, dry, and fold

- Washing takes 30 minutes
- Drying takes 40 minutes
- Folding takes 20 minutes
Sequential laundry takes 6 hours for 4 loads

Pipelined laundry takes 3.5 hours for 4 loads (start next task as soon as possible)
**Pipelining**: multiple tasks operating simultaneously using different resources.

- Pipelining doesn’t help latency of a single task, it helps throughput of the entire workload.
- Potential speed up equals the number of pipeline stages.

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**Pipeline rate is limited by slowest pipeline stage.**

- Time to “fill” pipeline and time to “drain” it reduces speed up.
- Stall pipeline to handle dependencies.
ISA Implementations

Instruction Set Architecture: the features of a microprocessor which are visible to the assembly language programmer.

Microarchitecture: the components and interconnections which implement an ISA.

Single-cycle ARM

The textbook discusses a single-cycle implementation of the ARM processor (each instruction executes in one clock cycle).

To simplify the diagrams, the processor only handles a few instructions: ADD, SUB, AND, ORR, LDR, STR, B

Also, it doesn’t allow shifts and has only limited options for immediate values
Single-cycle Datapath and Control

Utilize instruction-level parallelism:

- Divide single-cycle processor into 5 stages:
  - Fetch
  - Decode
  - Execute
  - Memory
  - Writeback
- Add pipeline registers between stages

Pipelined ARM
Pipelined Datapath and Control

Comparison

Single-Cycle

Pipelined
Single-Cycle

Instr 1 2
Fetch Instruction  
Dec Read Reg  
Execute ALU  
Memory Read/Write  
Wr Reg  

Instr 1 2 3
Fetch Instruction  
Dec Read Reg  
Execute ALU  
Memory Read/Write  
Wr Reg  

Pipelined

Instr 1 2 3
Fetch Instruction  
Dec Read Reg  
Execute ALU  
Memory Read/Write  
Wr Reg  

Instr 1 2 3
Fetch Instruction  
Dec Read Reg  
Execute ALU  
Memory Read/Write  
Wr Reg  

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1 2 3 4 5 6 7 8 9 10
Time (cycles)

LDR R2, [R0, #40]  
ADD R3, R9, R10  
SUB R4, R1, R5  
AND R5, R12, R13  
STR R6, [R1, #20]  
ORR R7, R11, #42  

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ARM Pipeline Changes

Early 3-stage version:

Recall that the assembler calculates branch offsets relative to the PC+8 – that’s a legacy of this early pipeline (the PC has been incremented by 4 twice when the 3rd stage is reached).

ARM Pipeline Changes

Classic 5-stage version:

Regardless of the number of pipeline stages, the last stage is the Writeback stage: if an instruction updates the register file, that happens in the last stage of the pipeline.
Evolution

- Deeper pipelines
- Superscalar (multiple pipelines)
- Multiple cores on same chip

MIPS R4400: 8 stages

![Diagram of MIPS R4400 Pipeline](Figure 1-2)
Superscalar: multiple pipelines

Figure 1-3 4-Way Superscalar Pipeline

Figure 1-4 Superscalar Pipeline Architecture in the R10000
CSE Pi Array

- Array of 22 boards
- Each board has a quad-core ARM Cortex-A7 processor
- Each board has 1 GB of RAM