Consider a circuit which functions as a specialized counter: it begins at seven and counts down to three (by ones), then starts over. That is, the circuit counts through the sequence:

<7, 6, 5, 4, 3, 7, 6, 5, 4, 3, ....>

The circuit uses D flip-flops to store the current value, and combinational logic to increment the current value. Assume that the circuit is initialized asynchronously (the initialization is independent of the combinational logic and can be ignored for this problem).

a) Give the truth table for the combinational component of this counter.

<table>
<thead>
<tr>
<th>current A B C</th>
<th>next A B C</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td></td>
</tr>
<tr>
<td>0 0 1</td>
<td></td>
</tr>
<tr>
<td>0 1 0</td>
<td></td>
</tr>
<tr>
<td>0 1 1</td>
<td></td>
</tr>
<tr>
<td>1 0 0</td>
<td></td>
</tr>
<tr>
<td>1 0 1</td>
<td></td>
</tr>
<tr>
<td>1 1 0</td>
<td></td>
</tr>
<tr>
<td>1 1 1</td>
<td></td>
</tr>
</tbody>
</table>

b) Give the Karnaugh maps for the combinational component of this counter. Then, give the minimized sum-of-products Boolean expressions for the combinational component of this counter.

\[
\begin{array}{ccc}
\text{A}\text{B}
\hline
\text{C} & 00 & 01 & 11 & 10 \\
0 & & & & \\
1 & & & & \\
\end{array}
\]

\[
\begin{array}{ccc}
\text{A}\text{B}
\hline
\text{C} & 00 & 01 & 11 & 10 \\
0 & & & & \\
1 & & & & \\
\end{array}
\]

\[
\begin{array}{ccc}
\text{A}\text{B}
\hline
\text{C} & 00 & 01 & 11 & 10 \\
0 & & & & \\
1 & & & & \\
\end{array}
\]