

CSE 320

Last name (printed): _____

Final Exam

First name (printed): _____

Form 3 X

Directions:

- a. DO NOT OPEN YOUR EXAM BOOKLET UNTIL YOU HAVE BEEN TOLD TO BEGIN.
- b. This exam booklet contains 40 questions, each of which will be weighted equally.
- c. You may use one 8.5" x 11" note sheet during the exam. No other reference materials or calculating devices may be used during the examination.
- d. Questions will not be interpreted during the examination.
- e. You should choose the single best alternative for each question, even if you believe that a question is ambiguous or contains a typographic error.
- f. Please fill in the requested information at the top of this exam booklet.
- g. Use a #2 pencil to encode any information on the OMR form.
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 - Last name and first initial
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- i. Please sign the OMR form.
- j. Only answers recorded on your OMR form will be counted for credit. Completely erase any responses on the OMR form that you wish to delete.
- k. You must turn in this exam booklet and the OMR form when you have completed the exam. When leaving, please be courteous to those still taking the exam.

```

*****
*   Final Exam Key                               *
*                                                                 *
* 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 *
*  D  E  A  C  B  A  E  A  C  E  B  D  C  C  A  D  C  C  E  D  B  C  B  B  *
*                                                                 *
* 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40             *
*  E  C  E  D  A  E  A  B  A  D  B  D  D  B  B  D                 *
*****

```

01. What combinational component does the following truth table represent?

A	B	C	D	E	F	G
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

- A) A decoder, where signals A and B are the control signals
- B) An encoder, where signals A and B are the control signals
- C) A multiplexer, where signal A is the data signal
- D) A demultiplexer, where signal A is the data signal
- E) None of the above.

02. What combinational component does the following truth table represent?

A	B	C	D	E
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

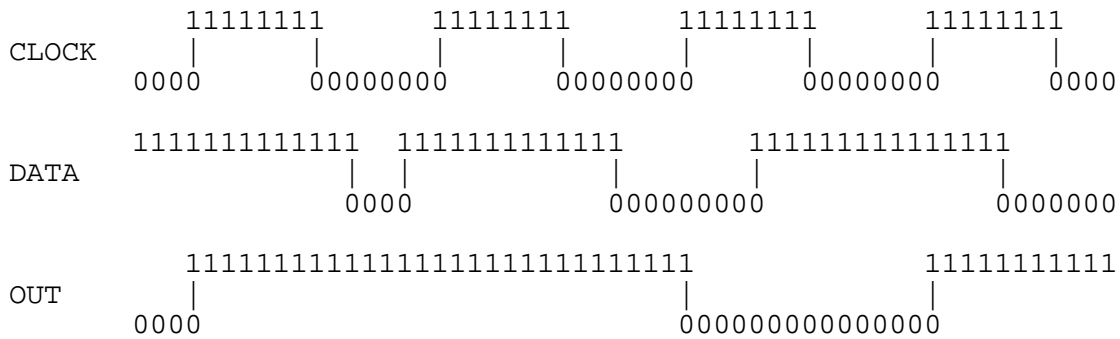
- A) A decoder, where signal A is the enable signal
- B) An encoder, where signal A is the enable signal
- C) A multiplexer, where signal A is the control signal
- D) A demultiplexer, where signal A is the control signal
- E) None of the above.

03. What combinational component does the following characteristic table represent?

A	B	C	D	E	F	G
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

- A) A priority encoder, where signal A has priority
- B) A multiplexer, where signal A is the control signal
- C) A demultiplexer, where signal A is the control signal
- D) A decoder, where signal A is the enable signal
- E) None of the above.

04. Consider the following timing diagram for a particular circuit. Assume that "CLOCK" and "DATA" represent the only two inputs to the circuit, and that "OUT" represents the only output signal.



What is the best characterization of this circuit?

- A) Combinational circuit
- B) Level-triggered sequential circuit
- C) Positive edge-triggered sequential circuit
- D) Negative edge-triggered sequential circuit
- E) None of the above.

05. What is the optimal expression for the following Boolean function (given as a minterm list)?

$$f(w,x,y,z) = m_1 + m_4 + m_5 + m_9 + m_{12} + m_{13} + m_{14}$$

- A) $xy'z' + y'z + wxyz'$
- B) $xy' + y'z + wxz'$
- C) $xy'z' + x'y'z + wxz'$
- D) $xy' + w'x'y'z + wx'y'z + wxyz'$
- E) None of the above.

```
#####  
# Figure 1 #  
#####
```

A circuit functions as a specialized three-bit counter, where the sequence of outputs from the circuit are: 000, 011, 110, 000, 011, 110, and so on.

The mapping of the current state to the next state uses the notation ABC, where A represents the most significant bit of the counter and C represents the least significant bit of the counter.

06. Consider the circuit described in Figure 1. Which of the following is the optimal expression for A?

- A) $A = C$
- B) $A = A'B$
- C) $A = A'BC$
- D) $A = C + AB' + A'B$
- E) None of the above.

07. Consider the circuit described in Figure 1. Which of the following is the optimal expression for B?

- A) $B = A' + B' + C$
- B) $B = A'B'C' + A'BC$
- C) $B = B'C' + BC$
- D) $B = B' + C$
- E) None of the above.

08. Consider the circuit described in Figure 1. Which of the following is the optimal expression for C?

- A) $C = B'$
- B) $C = A'B'$
- C) $C = A'B'C'$
- D) $C = B' + AC + A'C'$
- E) None of the above.

09. Consider a microprocessor which uses twelve-bit registers to hold signed integers and uses twos complement arithmetic. What are the largest and smallest signed integers which can be represented in a single register?

- A) +1023 (base 10) and -1024 (base 10)
- B) +1023 (base 10) and -1023 (base 10)
- C) +2047 (base 10) and -2048 (base 10)
- D) +2047 (base 10) and -2047 (base 10)
- E) None of the above.

10. Consider the 32-bit single precision floating point number whose internal representation is 00FFFFFF (in hexadecimal). Which of the following statements about that number is correct?

- A) The bit pattern represents zero.
- B) The bit pattern represents a denormal number.
- C) The bit pattern represents infinity.
- D) The bit pattern represents not-a-number.
- E) None of the above.

11. What is the 32-bit single precision internal representation (in hexadecimal) of the decimal value given below?

+0.625 (base 10)

- A) 7e400000 (base 16)
- B) 3f200000 (base 16)
- C) 7fa00000 (base 16)
- D) None of the above.
- E) 3fd00000 (base 16)

12. Consider the 64-bit double precision floating point number whose internal representation is FFFFFFFFFFFFFFFFFF (in hexadecimal). Which of the following statements about that number is correct?

- A) The bit pattern represents zero.
- B) The bit pattern represents a denormal number.
- C) The bit pattern represents infinity.
- D) The bit pattern represents not-a-number.
- E) None of the above.

13. What is the 64-bit double precision internal representation (in hexadecimal) of the decimal value given below?

-24.5 (base 10)

- A) c04c400000000000 (base 16)
- B) bfb8800000000000 (base 16)
- C) c038800000000000 (base 16)
- D) bfac400000000000 (base 16)
- E) None of the above.

```
#####  
# Figure 2 #  
#####
```

```
set    0xe60000c5, %g6  
set    0xba00003d, %g7  
  
addcc  %g6, %g7, %l0    ! Line 1  
  
sub    %g6, %g7, %l1  
sub    %g6, 0xff, %l2   ! Line 2  
  
and    %g6, %g7, %l3  
or     %g6, %g7, %l4   ! Line 3  
  
sra    %g6, 12, %l5  
srl    %g7, 8, %l6     ! Line 4
```

14. Consider the SPARC assembly language statements in Figure 2. Which of the following correctly lists the contents of the indicated register and the integer condition code bits after the statement labeled "Line 1" is executed?

- A) %l0: 9f0000f2 (base 16) NZVC: 1001 (base 2)
- B) %l0: 9f0000f2 (base 16) NZVC: 1010 (base 2)
- C) %l0: a0000102 (base 16) NZVC: 1001 (base 2)
- D) %l0: a0000102 (base 16) NZVC: 1010 (base 2)
- E) None of the above.

15. Consider the SPARC assembly language statements in Figure 2. Which of the following correctly lists the contents of the indicated registers after the statement labeled "Line 2" is executed?

- A) %l1: 2c000088 (base 16) %l2: e5ffffc6 (base 16)
- B) %l1: 2c000088 (base 16) %l2: e600003a (base 16)
- C) %l1: 3c000098 (base 16) %l2: e5ffffc6 (base 16)
- D) %l1: 3c000098 (base 16) %l2: e600003a (base 16)
- E) None of the above.

16. Consider the SPARC assembly language statements in Figure 2. Which of the following correctly lists the contents of the indicated registers after the statement labeled "Line 3" is executed?

- A) %l3: e200000d (base 16) %l4: 5c0000f8 (base 16)
- B) %l3: e200000d (base 16) %l4: fe0000fd (base 16)
- C) %l3: a2000005 (base 16) %l4: 5c0000f8 (base 16)
- D) %l3: a2000005 (base 16) %l4: fe0000fd (base 16)
- E) None of the above.

17. Consider the SPARC assembly language statements in Figure 2. Which of the following correctly lists the contents of the indicated registers after the statement labeled "Line 4" is executed?

- A) %l5: 000e6000 (base 16) %l6: 00ba0000 (base 16)
- B) %l5: 000e6000 (base 16) %l6: ffba0000 (base 16)
- C) %l5: fffe6000 (base 16) %l6: 00ba0000 (base 16)
- D) %l5: fffe6000 (base 16) %l6: ffba0000 (base 16)
- E) None of the above.

```
#####  
# Figure 3 #  
#####
```

```
set      0x456789ab, %g7  
  
set      LocA, %o0  
add      %o0, 16, %o1  
add      %o0, 12, %o2  
  
call     memory          ! Line 1  
nop  
  
! Output produced by the statement labeled "Line 1":  
!  
! 00021030: 44 55 66 77 88 99 aa bb cc dd ee ff 00 11 22 33  
  
ldsh     [%o0+6], %l0  
lduh     [%o0+6], %l1      ! Line 2  
  
ldsb     [%o0+3], %l2  
ldub     [%o0+3], %l3      ! Line 3  
  
sth      %g7, [%o2-4]  
stb      %g7, [%o2+1]  
  
call     memory          ! Line 4  
nop
```

18. Consider the SPARC assembly language statements in Figure 3. Which of the following correctly lists the contents of the indicated registers after the statement labeled "Line 2" is executed?

- A) %l0: 0000aabb (base 16) %l1: 0000aabb (base 16)
- B) %l0: 0000aabb (base 16) %l1: ffffaabb (base 16)
- C) %l0: ffffaabb (base 16) %l1: 0000aabb (base 16)
- D) %l0: ffffaabb (base 16) %l1: ffffaabb (base 16)
- E) None of the above.

19. Consider the SPARC assembly language statements in Figure 3. Which of the following correctly lists the contents of the indicated registers after the statement labeled "Line 3" is executed?

- A) %l2: 00000066 (base 16) %l3: 00000066 (base 16)
- B) %l2: 00000066 (base 16) %l3: fffffff66 (base 16)
- C) %l2: fffffff66 (base 16) %l3: 00000066 (base 16)
- D) %l2: fffffff66 (base 16) %l3: fffffff66 (base 16)
- E) None of the above.

20. Consider the SPARC assembly language statements in Figure 3. Which of the following is the output produced by the statement labeled "Line 4"?

- A) 00021030: 44 55 66 77 88 99 45 67 89 ab 45 67 89 ab 22 33
- B) 00021030: 44 55 66 77 88 99 00 00 89 ab 00 00 00 ab 22 33
- C) 00021030: 44 55 66 77 88 99 ff ff 89 ab ff ff ff ab 22 33
- D) 00021030: 44 55 66 77 88 99 aa bb 89 ab ee ff 00 ab 22 33
- E) None of the above.

21. Which of the following SPARC assembly language instructions is equivalent to the synthetic instruction "ret"?

- A) `jmp1 %r31+4, %r0`
- B) `jmp1 %r31+8, %r0`
- C) `jmp1 %r15+4, %r0`
- D) `jmp1 %r15+8, %r0`
- E) None of the above.

22. Consider the SPARC assembly language code segment below, where the "call" and the "nop" are the only instructions between the two comments.

```
! *** Line 1 ***  
  
    call sub  
    nop  
  
! *** Line 2 ***
```

Assuming that function "sub" obeys the SPARC subprogram conventions, which IU and FPU registers cannot be changed by calling "sub"? That is, list all IU and FPU registers which will contain the same values at "Line 1" and "Line 2".

- A) The FPU registers.
- B) The IU registers from the set `{%r0, ..., %r7}`.
- C) The IU registers from the set `{%r0, %r16, ..., %r31}`.
- D) All of the above.
- E) None of the above.

23. Consider the SPARC assembly language instructions shown below:

```
    .global exam  
    .section ".text"  
    .align 4  
exam:  
    save    %sp, -96, %sp  
  
    mov     %i2, %o0  
    add     %o0, 128, %o1  
    set     0x12345678, %o2  
    call    test  
    nop  
    st      %o0, [%i1]  
  
    ret  
    restore
```

Assume that the programmer wishes to move one instruction into the "call" instruction's delay slot. Which of the following instructions could be used for that purpose, without altering the behavior of function "exam"?

- A) The "mov" instruction
- B) The "add" instruction
- C) The "set" instruction
- D) All of the above.
- E) None of the above.

```
#####  
# Figure 4 #  
#####
```

```
double A, B = 5.0, C = 8.2, *D = &C;  
  
double test( double, double, double* );  
  
int main()  
{  
  A = test( B, C, D );  
}
```

24. Consider the C language statements in Figure 4. Assuming that function "test" obeys the SPARC subprogram conventions, where will function "test" find its first argument?

- A) In registers %r8 and %r9 of the IU.
- B) In registers %r24 and %r25 of the IU.
- C) In registers %f0 and %f1 of the FPU.
- D) In an eight-byte memory location.
- E) None of the above.

25. Consider the C language statements in Figure 4. Assuming that function "test" obeys the SPARC subprogram conventions, where will function "test" find its third argument?

- A) In registers %r12 and %r13 of the IU.
- B) In registers %r28 and %r29 of the IU.
- C) In registers %f0 and %f1 of the FPU.
- D) In an eight-byte memory location.
- E) None of the above.

26. Consider the C language statements in Figure 4. Assuming that function "test" obeys the SPARC subprogram conventions, where will function "test" place its return value before returning?

- A) In registers %r8 and %r9 of the IU.
- B) In registers %r24 and %r25 of the IU.
- C) In registers %f0 and %f1 of the FPU.
- D) In an eight-byte memory location.
- E) None of the above.

```
#####  
# Figure 5 #  
#####
```

```
int X, Y;  
  
if (X < 40 || Y > 80)  
{  
    X = Y;  
}
```

27. Consider the C language statements in Figure 5. Assume the task is to be implemented in SPARC assembly language instead of C. An outline of the assembly language sequence is given below:

```
set    X, %i0  
ld     [%i0], %l0  
set    Y, %i1  
ld     [%i1], %l1  
  
! *** Line 1 ***  
  
endif:
```

Which of the following statement sequences is a valid replacement for the comment "*** Line 1 ***" in the sequence?

- A)

```
cmp    %l0, 40  
bl     endif  
nop  
cmp    %l1, 80  
bg     endif  
nop  
st     %l0, [%i1]
```
- B)

```
cmp    %l0, 40  
bge    endif  
nop  
cmp    %l1, 80  
ble    endif  
nop  
st     %l0, [%i1]
```
- C)

```
cmp    %l0, 40  
bg     endif  
nop  
cmp    %l1, 80  
bl     endif  
nop  
st     %l0, [%i1]
```
- D)

```
cmp    %l0, 40  
ble    endif  
nop  
cmp    %l1, 80  
bge    endif  
nop  
st     %l0, [%i1]
```
- E) None of the above.

```
#####  
# Figure 6 #  
#####
```

```
struct Student  
{  
    char Name[25];  
    int ID;  
    int Points;  
};  
  
int exam( struct Student List[], int I )  
{  
    return List[I].ID;  
}
```

28. Consider the C language statements in Figure 6. Assume function "exam" is to be implemented in SPARC assembly language instead of C. A stub for function "exam" is given below:

```
        .global exam  
        .section ".text"  
        .align 4  
exam:  
        save    %sp, -96, %sp  
  
        ! *** Line 1 ***  
  
        ret  
        restore
```

Which of the following statement sequences is a valid replacement for the comment "*** Line 1 ***" in function "exam"?

- A)

```
smul    %i1, 29, %l1  
add     %i0, %l1, %l0  
ld      [%l0+25], %i0
```
- B)

```
smul    %i1, 30, %l1  
add     %i0, %l1, %l0  
ld      [%l0+26], %i0
```
- C)

```
smul    %i1, 33, %l1  
add     %i0, %l1, %l0  
ld      [%l0+25], %i0
```
- D)

```
smul    %i1, 36, %l1  
add     %i0, %l1, %l0  
ld      [%l0+28], %i0
```
- E) None of the above.

Figure 7 #
#####

The following symbol table was constructed by an assembler from the SPARC assembly language source file named "final.s".

Symbol	Value	Abs/Rel	Local/Global
endloop	.text+00000284	Rel	Local
max	00000007	Abs	Local
verify	.text+00000008	Rel	Local

29. Consider the symbol table in Figure 7 and the SPARC assembly language statement shown below. Assuming that it is contained in "final.s" at the relative address shown, what will be the object code for that statement?

```
(text+0x0004):  xorcc  %l5, %o2, %i3
```

- A) b69d400a (base 16)
- B) aa9a801b (base 16)
- C) b69d600a (base 16)
- D) aa9aa01b (base 16)
- E) None of the above.

30. Consider the symbol table in Figure 7 and the SPARC assembly language statement shown below. Assuming that it is contained in "final.s" at the relative address shown, what will be the object code for that statement?

```
(text+0x0008):  stb  %g6, [%l4+max]
```

- A) e829a000 (base 16)
- B) e8298000 (base 16)
- C) e829a007 (base 16)
- D) e8298007 (base 16)
- E) None of the above.

31. Consider the symbol table in Figure 7 and the SPARC assembly language statement shown below. Assuming that it is contained in "final.s" at the relative address shown, what will be the object code for that statement?

```
(text+0x0034):  bcs  verify
```

- A) 0abffff5 (base 16)
- B) 0a00000b (base 16)
- C) 0abfffd4 (base 16)
- D) 0a00002c (base 16)
- E) None of the above.

32. Consider the symbol table in Figure 7 and the SPARC assembly language statement shown below. Assuming that it is contained in "final.s" at the relative address shown, what will be the object code for that statement?

```
(text+0x0050):  ba  endloop
```

- A) 10cfff73 (base 16)
- B) 1080008d (base 16)
- C) 10cffdcc (base 16)
- D) 10800234 (base 16)
- E) None of the above.

Figure 8 #
#####

The contents of the control and general-purpose registers are shown below (in hexadecimal) at the end of the fetch phase of the instruction cycle for a single-cycle (non-pipelined) implementation of the ARC+ microprocessor.

nPC: 00012004 PC: 00012000 PSR: 00A00000 ICC: A (N-V-)

R[00]: 00000000 R[08]: 08080808 R[10]: 10101010 R[18]: 18181818
R[01]: 01010101 R[09]: 09090909 R[11]: 11111111 R[19]: 19191919
R[02]: 02020202 R[0A]: 0A0A0A0A R[12]: 12121212 R[1A]: 1A1A1A1A
R[03]: 03030303 R[0B]: 0B0B0B0B R[13]: 13131313 R[1B]: 1B1B1B1B
R[04]: 04040404 R[0C]: 0C0C0C0C R[14]: 14141414 R[1C]: 1C1C1C1C
R[05]: 05050505 R[0D]: 0D0D0D0D R[15]: 15151515 R[1D]: 1D1D1D1D
R[06]: 06060606 R[0E]: 0E0E0E0E R[16]: 16161616 R[1E]: 1E1E1E1E
R[07]: 07070707 R[0F]: 0F0F0F0F R[17]: 17171717 R[1F]: 1F1F1F1F

33. Consider the information in Figure 8. If the IR currently contains the value A01D0006 (base 16), what will be the output of MUX-B?

- A) 12121212 (base 16)
- B) 1A1A1A1A (base 16)
- C) EDEDEDED (base 16)
- D) 00012000 (base 16)
- E) None of the above.

34. Consider the information in Figure 8. If the IR currently contains the value 4000001C (base 16), what will be the output of MUX-B?

- A) 0F0F0F0F (base 16)
- B) 1F1F1F1F (base 16)
- C) 1F1F1F2B (base 16)
- D) 00012000 (base 16)
- E) None of the above.

35. Consider the information in Figure 8. If the IR currently contains the value 212242AF (base 16), what will be the output of MUX-B?

- A) 10101010 (base 16)
- B) 890ABC00 (base 16)
- C) 002242AF (base 16)
- D) 00012000 (base 16)
- E) None of the above.

36. Consider the information in Figure 8. If the IR currently contains the value 9FC52008 (base 16), what will be the output of MUX-B?

- A) 1414141C (base 16)
- B) 14141414 (base 16)
- C) 0F0F0F17 (base 16)
- D) 00012000 (base 16)
- E) None of the above.

Figure 9 #
#####

The contents of the control and general-purpose registers are shown below (in hexadecimal) at the end of the fetch phase of the instruction cycle for a single-cycle (non-pipelined) implementation of the ARC+ microprocessor.

nPC: 00012004 PC: 00012000 PSR: 00A00000 ICC: A (N-V-)

R[00]: 00000000 R[08]: 08080808 R[10]: 10101010 R[18]: 18181818
R[01]: 01010101 R[09]: 09090909 R[11]: 11111111 R[19]: 19191919
R[02]: 02020202 R[0A]: 0A0A0A0A R[12]: 12121212 R[1A]: 1A1A1A1A
R[03]: 03030303 R[0B]: 0B0B0B0B R[13]: 13131313 R[1B]: 1B1B1B1B
R[04]: 04040404 R[0C]: 0C0C0C0C R[14]: 14141414 R[1C]: 1C1C1C1C
R[05]: 05050505 R[0D]: 0D0D0D0D R[15]: 15151515 R[1D]: 1D1D1D1D
R[06]: 06060606 R[0E]: 0E0E0E0E R[16]: 16161616 R[1E]: 1E1E1E1E
R[07]: 07070707 R[0F]: 0F0F0F0F R[17]: 17171717 R[1F]: 1F1F1F1F

37. Consider the information in Figure 9. If the IR currently contains the value 4000001C (base 16), what will be the output of MUX-C?

- A) 00012000 (base 16)
- B) 00012008 (base 16)
- C) 0001201C (base 16)
- D) 00012070 (base 16)
- E) None of the above.

38. Consider the information in Figure 9. If the IR currently contains the value 0A80000D (base 16), what will be the output of MUX-C?

- A) 00012000 (base 16)
- B) 00012008 (base 16)
- C) 0001200D (base 16)
- D) 00012034 (base 16)
- E) None of the above.

39. Consider the information in Figure 9. If the IR currently contains the value A134A010 (base 16), what will be the output of MUX-C?

- A) 00012000 (base 16)
- B) 00012008 (base 16)
- C) 0001202D (base 16)
- D) 000120B4 (base 16)
- E) None of the above.

40. Consider the information in Figure 9. If the IR currently contains the value 0E800007 (base 16), what will be the output of MUX-C?

- A) 00012000 (base 16)
- B) 00012007 (base 16)
- C) 00012008 (base 16)
- D) 0001201C (base 16)
- E) None of the above.