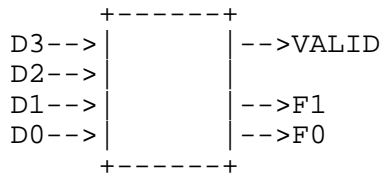


CSE 320 Sample Exam #1

1. (15 pts) Consider the following component-level diagram of a 4-to-2 priority encoder with a "valid output" signal, where D3 is the highest priority input signal.



When all four of the input signals are deasserted (the logical value zero), the "VALID" signal is deasserted and the other two output signals are both irrelevant. Otherwise, the "VALID" signal is asserted (the logical value one) and the priority encoder performs its normal encoding operation.

a) Describe the functionality of this priority encoder using a truth table or a characteristic table.

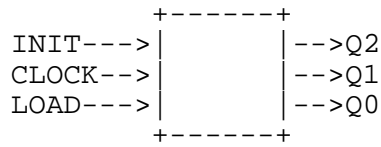
D3	D2	D1	D0	Valid	F1	F0
0	0	0	0	0	X	X
0	0	0	1	1	0	0
0	0	1	X	1	0	1
0	1	X	X	1	1	0
1	X	X	X	1	1	1

b) Give a gate-level diagram of this priority encoder.

A correct response would include a circuit diagram for all three functions, based on the Boolean expressions:

$$\begin{aligned}
 \text{Valid} &= D3 + D2 + D1 + D0 \\
 F1 &= D3 + D3'D2 \\
 F0 &= D3 + D3'D2'D1
 \end{aligned}$$

2. (10 pts) Consider the following component-level diagram of a three-bit sequencer which generates the outputs 001, 010, 100, 001, 010, 100, and so on.



The three "Q" output signals always reflect the current contents of the sequencer.

When the asynchronous "INIT" signal is asserted, the sequencer is initialized (the "Q0" output signal is asserted, while the "Q1" and "Q2" output signals are deasserted).

When the "LOAD" signal and the "CLOCK" signal are both asserted, the sequencer performs its shift operation.

Draw a gate-level diagram of this sequencer. You may assume the existence of gates from the set {NOT, AND, OR} and D flip-flops (you do not need to show the "insides" of those gates or flip-flops). Also, you may assume that the flip-flops have asynchronous "SET" and "RESET" inputs, as well as "DATA" and "CLOCK" inputs.

A correct response would include a circuit diagram with one AND gate and three DFFs.

The INIT signal would be connected to the SET input on DFF0 and to the RESET input on DFF1 and DFF2.

The CLOCK and LOAD signals would be connected to the AND gate. The output of the AND gate would be connected to the CLOCK input on all three DFFs.

The Q output of DFF0 would be connected to the DATA input of DFF1. The Q output of DFF1 would be connected to the DATA input of DFF2. The Q output of DFF2 would be connected to the DATA input of DFF0.

3. (15 pts) Consider a circuit which functions as a specialized counter: it begins at one and counts up by two (modulo eight). Recall that seven plus two equals one in modulo eight arithmetic.

The circuit uses D flip-flops to store the current value, and combinational logic to increment the current value. Assume that the circuit is initialized asynchronously (the initialization is independent of the combinational logic and can be ignored for this problem).

a) Give the truth table for the combinational component of this counter.

Current			Next		
Q2	Q1	Q0	Q2	Q1	Q0
0	0	0	X	X	X
0	0	1	0	1	1
0	1	0	X	X	X
0	1	1	1	0	1
1	0	0	X	X	X
1	0	1	1	1	1
1	1	0	X	X	X
1	1	1	0	0	1

b) Give the Karnaugh maps for the combinational component of this counter.

Next Q2

	00	01	11	10	
0	X	0	1	X	(with the appropriate entries circled)
1	X	1	0	X	

Next Q1

	00	01	11	10	
0	X	1	0	X	(with the appropriate entries circled)
1	X	1	0	X	

Next Q0

	00	01	11	10	
0	X	1	1	X	(with the appropriate entries circled)
1	X	1	1	X	

c) Give the minimized expressions for the combinational component of this counter.

$$\begin{aligned} \text{Next } Q2 &= Q2 Q1' + Q2' Q1 \\ \text{Next } Q1 &= Q1' \\ \text{Next } Q0 &= 1 \end{aligned}$$

4. (10 pts) Suppose that a machine uses ten-bit registers to hold signed integers and uses twos complement arithmetic.

a) What is the largest signed number that can be represented? Give your answer in both binary and decimal.

Binary: 0111111111_____

Decimal: +511_____

b) What is the smallest signed number that can be represented? Give your answer in both binary and decimal.

Binary: 1000000000_____

Decimal: -512_____

c) Give the internal representation of each of the following decimal numbers.

+139: 0010001011_____

-161: 1101011111_____

5. (16 pts) Consider the following C program. In the space provided, give the hexadecimal value which will be displayed by each call to "printf".

```
#include <stdio.h>

int main()
{
    int aaa = 0x9c00007e;
    int bbb = 0x5d0000b4;

    printf( "%08x\n", ~aaa );           /* __63FFFF81_____ */
    printf( "%08x\n", aaa & bbb );     /* __1C000034_____ */
    printf( "%08x\n", aaa | bbb );     /* __DD0000FE_____ */
    printf( "%08x\n", aaa ^ bbb );     /* __C10000CA_____ */
    printf( "%08x\n", aaa << 20 );     /* __07E00000_____ */
    printf( "%08x\n", aaa >> 16 );     /* __FFFF9C00_____ */
    printf( "%08x\n", bbb << 12 );     /* __000B4000_____ */
    printf( "%08x\n", bbb >> 8 );      /* __005D0000_____ */
}
```

6. (8 pts) Suppose that a machine uses eight bits to represent signed integers, uses twos complement arithmetic, and has the integer condition codes discussed at lecture. For each of the problems below, give the result (in binary) of the addition as it would be performed by this machine, and give the value of the indicated condition code bits after the operation is complete.

a) Sum of the eight-bit operands (given in binary).

11101001	Sum: <u> 10011110 </u>
ADD 10110101	N: <u> 1 </u> Z: <u> 0 </u> V: <u> 0 </u> C: <u> 1 </u>

b) Sum of the eight-bit operands (given in binary).

11100110	Sum: <u> 01111011 </u>
ADD 10010101	N: <u> 0 </u> Z: <u> 0 </u> V: <u> 1 </u> C: <u> 1 </u>

7. (4 pts) Consider the following list of terms associated with IEEE floating point representation.

- Infinity
- NaN
- Zero
- Denormal
- Normalized

For each single-precision floating point number shown below (in hexadecimal), state the term from the list above which best describes that number.

- 70033334 Normalized
- 803d0000 Denormal
- a9600000 Normalized
- ff880000 NaN

8. (12 pts) The following questions refer to IEEE floating point numbers. Show your work for possible partial credit.

a) Give the 64-bit double precision internal representation (in hexadecimal) of the decimal value given below.

-0.375 BFD8000000000000

b) Give the decimal value of the 64-bit double precision floating point number whose internal representation is given below (in hexadecimal).

404CA00000000000 +57.25

c) Give the 32-bit single precision internal representation (in hexadecimal) of the decimal value given below.

+5.875 40BC0000